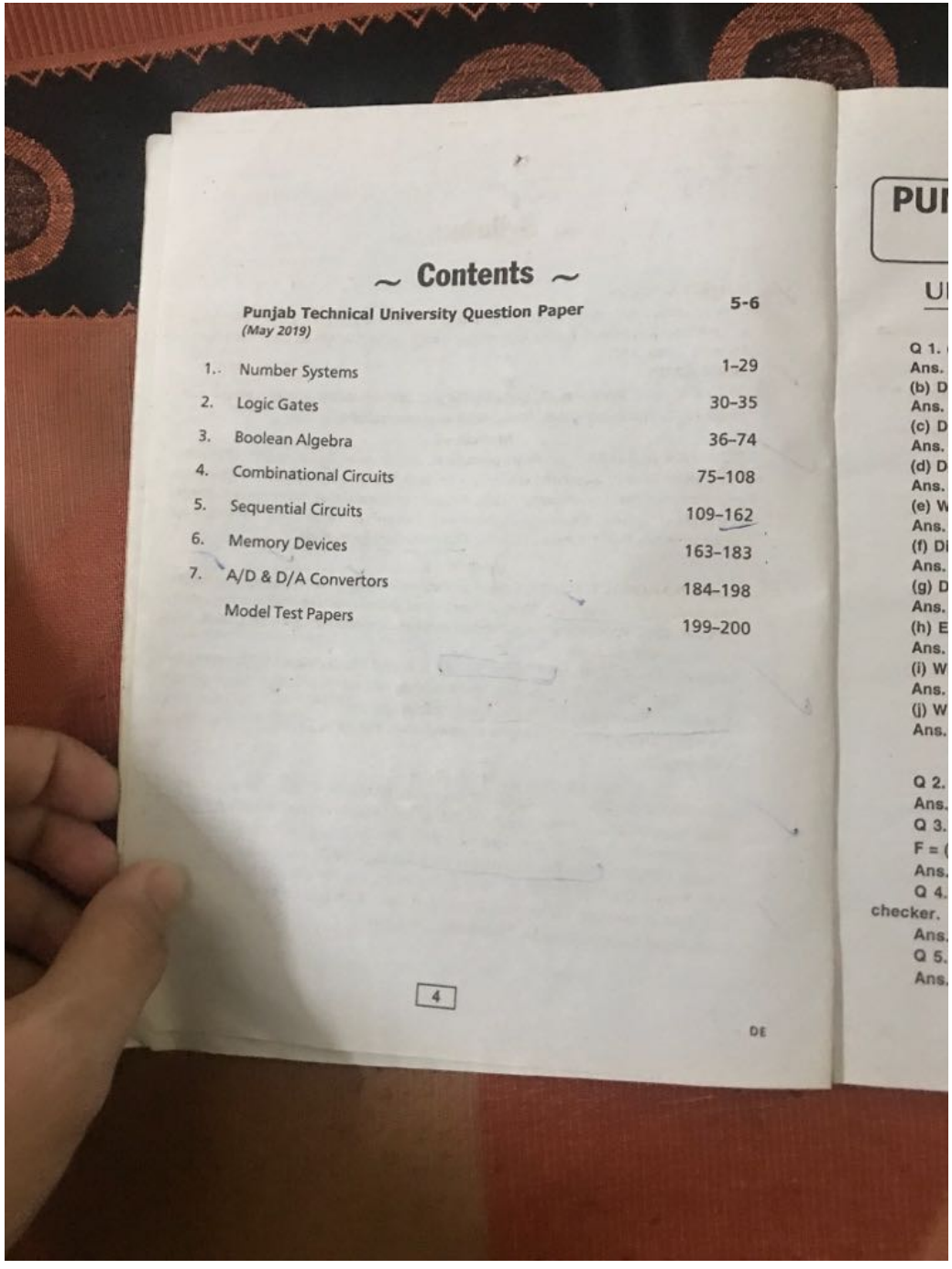

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PUNJAB TECHNICAL UNIVERSITY QUESTION PAPERS

UNIVERSITY QUESTION PAPER, MAY–2019

SECTION – A

Q 1. (a) Multiply 1011.01 with 110.1.

Ans. *Refer to Chapter No. 1 Q.No. 76*

(b) Discuss the principle of duality.

Ans. *Refer to Chapter No. 3 Q.No. 49*

(c) Distinguish between combination and sequential logic circuits.

Ans. *Refer to Chapter No. 5 Q.No. 15*

(d) Define R-2R ladder DAC.

Ans. *Refer to Chapter No. 7 Q.No. 26*

(e) What is the purpose of state diagram ?

Ans. *Refer to Chapter No. 5 Q.No. 82*

(f) Discuss race around condition in JK flip flop.

Ans. *Refer to Chapter No. 5 Q.No. 55*

(g) Draw logic diagram of 3-line to 8-line decoder.

Ans. *Refer to Chapter No. 4 Q.No. 53*

(h) Explain level triggering.

Ans. *Refer to Chapter No. 5 Q.No. 67*

(i) What is serial-out shift register ?

Ans. *Refer to Chapter No. 5 Q.No. 38*

(j) Write short note on Programmable Logic Arrays.

Ans. *Refer to Chapter No. 6 Q.No. 15*

SECTION – B

Q 2. What is the importance, applications and uses of Gray code?

Ans. *Refer to Chapter No. 1 Q.No. 61*

Q 3. Solve the following Boolean functions by using K-map.

$F = (W, X, Y, Z) = \sum (0, 1, 4, 5, 6, 8, 9, 10, 12, 13, 14)$

Ans. *Refer to Chapter No. 3 Q.No. 57*

Q 4. With a neat block diagram explain the function of encoder. Explain parity checker.

Ans. *Refer to Chapter No. 4 Q.No. 54*

Q 5. Discuss the advantages and disadvantages of TTL Logic Family.

Ans. *Out of syllabus*

rth complement = $r^n - N$ for $N \neq 0$
= 0 for $N = 0$

Alternately, it is defined as

rth's complement of a positive number N = its (rth's – 1) complement + 1

i.e. (rth's – 1) complement
+ 1
rth's complement (for positive number 'N')

- Numbers without +ve/–ve sign are unsigned numbers.
- Numbers represented by sign magnitude are signed numbers.
- BCD represent as 4 -bit binary code; also known as 8421 code.
- Excess-3 code is obtained by addition of three i.e. $(0011)_2$ to BCD and is self complementary.
- Gray codes are reflected codes in which the successive coded characters differ in only 1 bit position.
- Alphanumeric codes are represented by letters, symbols and numbers. These are ABCII codes, EBCDIC codes and ICII code.

QUESTION-ANSWERS

Q 1. What is number system? What are its types? Give example for each type of number system.

Ans. Number system : It is a set of rules and symbols, used to represent numbers. The number system can be classified into weighted or positinal and non-weighted or non-positinal systems. Most of the number systems are of weighted type.

The knowledge of number system is very essential because the design and organisation of a computer is dependent upon the number systems. Few important points related to number system are :

1. Base or Radix : It is defined as the number of different symbols used in the number system. The number of values that a character or digit can assume is called the Radix or Base of the system.

2. The largest value of a digit is always less than the Radix or Base : If Radix or Base is represented by 'r' or 'b', then the largest value of a digit is given by (r – 1) or (b – 1).

For e.g. The largest digit in decimal number system is (10 – 1) = 9. Where, 10 is the radix of decimal number system.

Types of Number System : Following table shows the various number system with their radix (r) or base (b).

Type of Number	Radix or Base
Binary	2
Octal	8
Decimal	10
Hexadecimal	16

Chapter 1

Number Systems

Contents

Binary, Octal, Decimal, Hexadecimal. Number base conversions, 1's, 2's complements, signed Binary numbers. Binary Arithmetic, Binary codes: Weighted BCD, Gray code, Excess 3 code, ASCII.

POINTS TO REMEMBER

- There are two input signals : **analog signals** have infinite number of distinct values and are contious, while **digital signals** have finite number of distinct values and are discrete in nature.
- Types of number systems are : decimal, binary, octal, hexadecimal.
- Codes are representation of digital in specified format which include symbols, alphabets etc.
- There are two logic levels in digital system : high (1) and low (0).
- There are two logic systems : positive and negative.
- Number system is a set of rules and symbols to represent numbers. It can be weighted or non-weighted.
- Number of values that a character or digit can assume is called Radix or Base.
- Decimal number system has radix '10'. Leftmost digit is MSD and rightmost digit is LSD.
- Binary number system has radix '2' and two binary digits one '1' and '0'. Its weight is expressed as a power of 2.
- The smallest unit of information is called bit (0 and 1).
- Binary representation of four bits is called a Nibble.
- A byte is a combination of 8-binary bits.
- A word is a combination of 16-binary bits.
- Octal numbers system has radix '8' of the digits are (0 to 7). Its weight is expressed in power of 8.
- Hexadecimal has radix '16'. The digits are 0 to 9 in continuation with letters A to F. Its weight is expressed in power of 16.
- 1's complement of a binary number is written by simply replacing all 0's by 1 and all 1's by 0.
- 2's complement is one increment of 1's complement.
- **rth's complement :** For a given positive number 'N' having radix 'r' or base 'r' with 'n' number of digits in integer part and 'm' number of digits in fractional part, the number 'N' for rth's complement in defined as

Q 6. How does a Dynamic RAM cell works ? Write its applications.

Ans. *Refer to Chapter No. 6 Q.No. 44*

SECTION – C

Q 7. (a) What are Mealy and Moore models of sequential circuits ?

Ans. *Refer to Chapter No. 5 Q.No. 83*

(b) Give the introduction of Quine-McCluskey method of minimization.

Ans. *Refer to Chapter No. 3 Q.No. 58*

Q 8. Explain the types of counter. Write the steps to design a Synchronous Counter using JK flip flops.

Ans. *Refer to Chapter No. 5 Q.No. 84*

Q 9. What are the types of analog to digital converter techniques ? Explain any one in detail.

Ans. *Refer to Chapter No. 7 Q.No. 15 & 19*

❑❑❑

CONVERSION OF DIFFERENT NUMBERS

(I) CONVERSION FROM BINARY TO DECIMAL.

Q 1. Convert the binary number $(110)_2$ to its decimal equivalent.

Solution. $(110)_2 = 1 \times 2^2 + 1 \times 2^1 + 0 \times 2^0$

$= 4 + 2 + 0 = 6$

$(110)_2 = (6)_{10}$

Q 2. Convert the binary number (1011.01) to its decimal equivalent.

Solution. $(1011.01)_2 = 1 \times 2^3 + 0 \times 2^2 + 1 \times 2^1 + 1 \times 2^0 \times 0 \times 2^{-1} + 1 \times 2^{-2}$

$= 8 + 0 + 2 + 1.0 + 0.25 = 11.25$

$(1011.01)_2 = (11.25)_{10}$

Q 3. Convert the following :

$(11011.111)_2 = (?)_{10}$

Solution. $(11011.111)_2 = 1 \times 2^4 + 1 \times 2^3 + 0 \times 2^2 + 1 \times 2^1 + 1 \times 2^0 + 1 \times 2^{-1}$

$+ 1 \times 2^{-2} + 1 \times 2^{-3}$

$= 16 + 8 + 0 + 2 + 1 + 0.5 + 0.25 + 0.125$

$= (27.875)_{10}$

$(11011.111)_2 = (27.875)_{10}$

(II) CONVERSION FROM OCTAL TO DECIMAL.

Q 4. Convert the following :

$(71)_8 = (?)_{10}$

Solution. $(71)_8 = 7 \times 8^1 + 1 \times 8^0$

$= 56 + 1$

$= 57$

$(71)_8 = (57)_{10}$

Q 5. Convert the following :

$(521.63)_8 = (?)_{10}$

Solution. $(521.63)_8 = 5 \times 8^2 + 2 \times 8^1 + 1 \times 8^0 + 6 \times 8^{-1} + 3 \times 8^{-2}$

$= 320 + 16 + 1 + 0.75 + 0.0468$

$= 337.7968$

$(521.63)_8 = (337.7968)_{10}$

Q 6. Convert the following :

$(385.24)_8 = (?)_{10}$

Solution. $(385.24)_8 = 3 \times 8^2 + 8 \times 8^1 + 5 \times 8^0 + 2 \times 8^{-1} + 4 \times 8^{-2}$

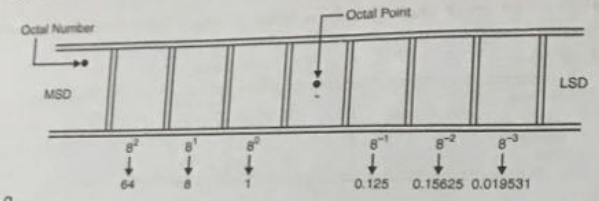
$= 192 + 48 + 5 + 0.25 + 0.0625$

$= 245.3125$

$(385.24)_8 = (245.3125)_{10}$

It make use of first eight digits of decimal number system i.e. 0, 1, 2, 3, 4, 5, 6 and 7. Thus, 8 and 9 digits never come in octal number system.

Octal positions values as a power of 8 are as shown :



e.g.

$N = (431.32)_8$, find its decimal equivalent

$= 4 \times 8^2 + 3 \times 8^1 + 1 \times 8^0 + 3 \times 8^{-1} + 2 \times 8^{-2}$

$= 4 \times 64 + 3 \times 8 + 1 \times 1 + \frac{3}{8} + \frac{2}{64}$

$= 256 + 24 + 1 + 0.375 + 0.03125$

$N = (281.40625)_{10}$

$N = (431.32)_8 = (281.40625)_{10}$

4. Hexadecimal Number System : The number system having radix or base '16' is called as hexadecimal number system. In short these are known as hex system. The number of values assumed by each digit are 0 through 9 and letters A, B, C, D, E and F. Thus the sixteen possible values are

0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F,

Here 'A' represents 10
'B' represents 11
'C' represents 12
'D' represents 13
'E' represents 14
'F' represents 15

The largest value or maximum value for the system is

$(r - 1) = (16 - 1) = 15$

e.g.

$N = (3FB)_{16}$, find its decimal equivalent

$= 3 \times 16^2 + F \times 16^1 + B \times 16^0$

$= 3 \times 256 + 15 \times 16 + 11 \times 1$

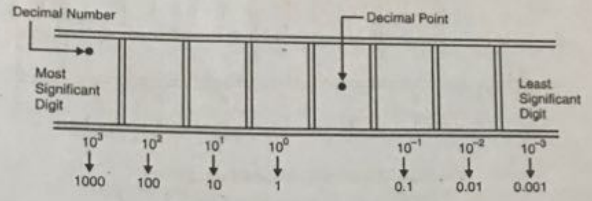
$= 768 + 250 + 11$

$= (1019)_{10}$

$N = (3FB)_{16} = (1019)_{10}$

1. The Decimal Number System : The number system having radix or base '10' is called as decimal number system. The number which we make use in our life is called the decimal number system.

The decimal system has the base value of 10. So, its maximum or largest value of a digit is $(r - 1) = 10 - 1 = 9$, where r = radix or base. Decimal position values as powers of 10 are as shown :



e.g. $N = (786.182)_{10}$

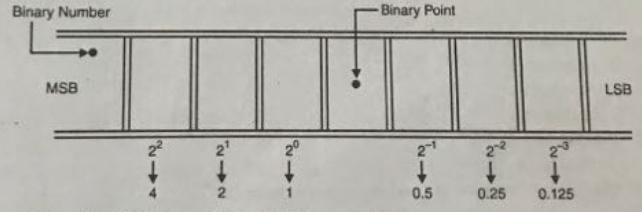
$$(786.182)_{10} = 7 \times 10^2 + 8 \times 10^1 + 6 \times 10^0 + 1 \times 10^{-1} + 8 \times 10^{-2} + 2 \times 10^{-2}$$

2. Binary Number System : The number system having radix or base '2' is called as binary number system.

As the radix or base value of binary number system is '2', so its maximum value of digit is :

$$(r - 1) = (2 - 1) = 1, \text{ where r is radix or base.}$$

The two binary digits are '1' and '0'. In binary system each binary digit is known as bit and has its own weight or value. Its weight is expressed as a power of 2.



e.g. $N = (1100.011)_2$, find its decimal equivalent.

$$1 \times 2^3 + 1 \times 2^2 + 0 \times 2^1 + 0 \times 2^0 + 0 \times 2^{-1} + 1 \times 2^{-2} + 1 \times 2^{-3}$$

$$= 8 + 4 + 0 + 0 + 0.25 + 0.125$$

$$N = (12.375)_{10}$$

So $N = (1100.011)_2 = (12.375)_{10}$

3. Octal Number System : The number system which make use of radix '8' is known as octal number system. As the radix or base of octal number system is '8', so its maximum or largest value of a digit is

$(r - 1) = (8 - 1) = 7$ where r is radix or base.

(VI) CONVERSION FROM DECIMAL TO HEX.

Q 16. Convert $(80)_{10} = (?)_{16}$

Solution.

16	80	
16	5	0
	0	5

LSD ↑ MSD

$(80)_{10} = (50)_{16}$

Q 17. Convert $(0.122)_{10} = (?)_{16}$

Solution.

	Curry	Hex
$0.122 \times 16 = 1.952$	1	1
$0.952 \times 16 = 15.232$	16	F
$0.232 \times 16 = 3.712$	3	3
$0.712 \times 16 = 11.392$	11	B
$0.392 \times 16 = 6.272$	6	6
$0.272 \times 16 = 4.352$	4	4

MSD ↓ LSD

$(0.122)_{10} \rightarrow (0.1F3B64)_{16}$

Q 18. Convert $(7825.760)_{10} \rightarrow (?)_{16}$

Solution.

16	7825	
16	489	1
16	30	9
16	1	14
	0	1

LSD ↑ MSD

Here, 14 = E

$(7825)_{10} = (1E91)_{16}$

$0.760 \times 16 = 12.16$ → $12 \rightarrow C$

$0.16 \times 16 = 2.56$ → 2

$0.56 \times 16 = 8.96$ → $8 \rightarrow 8$

$0.96 \times 16 = 15.36$ → $15 \rightarrow F$

$(0.760)_{10} = (0.C28F)_{16}$

$(7825.760)_{10} = (1E91.C28F)_{16}$.

(VII) CONVERSION FROM BINARY TO OCTAL.

Q 19. Convert $(10110)_2 \rightarrow (?)_8$

Solution. $10110 = \underbrace{010}_{2}\ \underbrace{110}_{6}$

$(10110)_2 = (26)_8$

Q 12. $(0.6875)_{10} \rightarrow (?)_2$

Solution.

$0.6875 \times 2 = 1.3750$	1	MSB
$0.3750 \times 2 = 0.7500$	0	↓
$0.7500 \times 2 = 1.5000$	1	↓
$0.5000 \times 2 = 1.0000$	1	LSB

$(0.6875)_{10} = (0.1011)_2$

(V) CONVERSION DECIMAL TO OCTAL

Q 13. Convert $(241)_{10} = (?)_8$

Solution.

8	241		
8	30	1	LSD ↑
8	3	6	
	0	3	MSD

$(241)_{10} = (361)_8$

Q 14. Convert $(0.6234)_{10} \rightarrow (?)_8$

Solution.

$0.6234 \times 8 = 4.9872$	4	MSD
$0.9872 \times 8 = 7.8976$	7	↓
$0.8976 \times 8 = 7.1808$	7	↓
$0.1808 \times 8 = 1.4484$	1	↓
$0.4484 \times 8 = 3.5712$	3	LSD

$(0.6234)_{10} = (0.47713)_8$

Q 15. Convert $(305.6875)_{10} = (?)_8$

Solution.

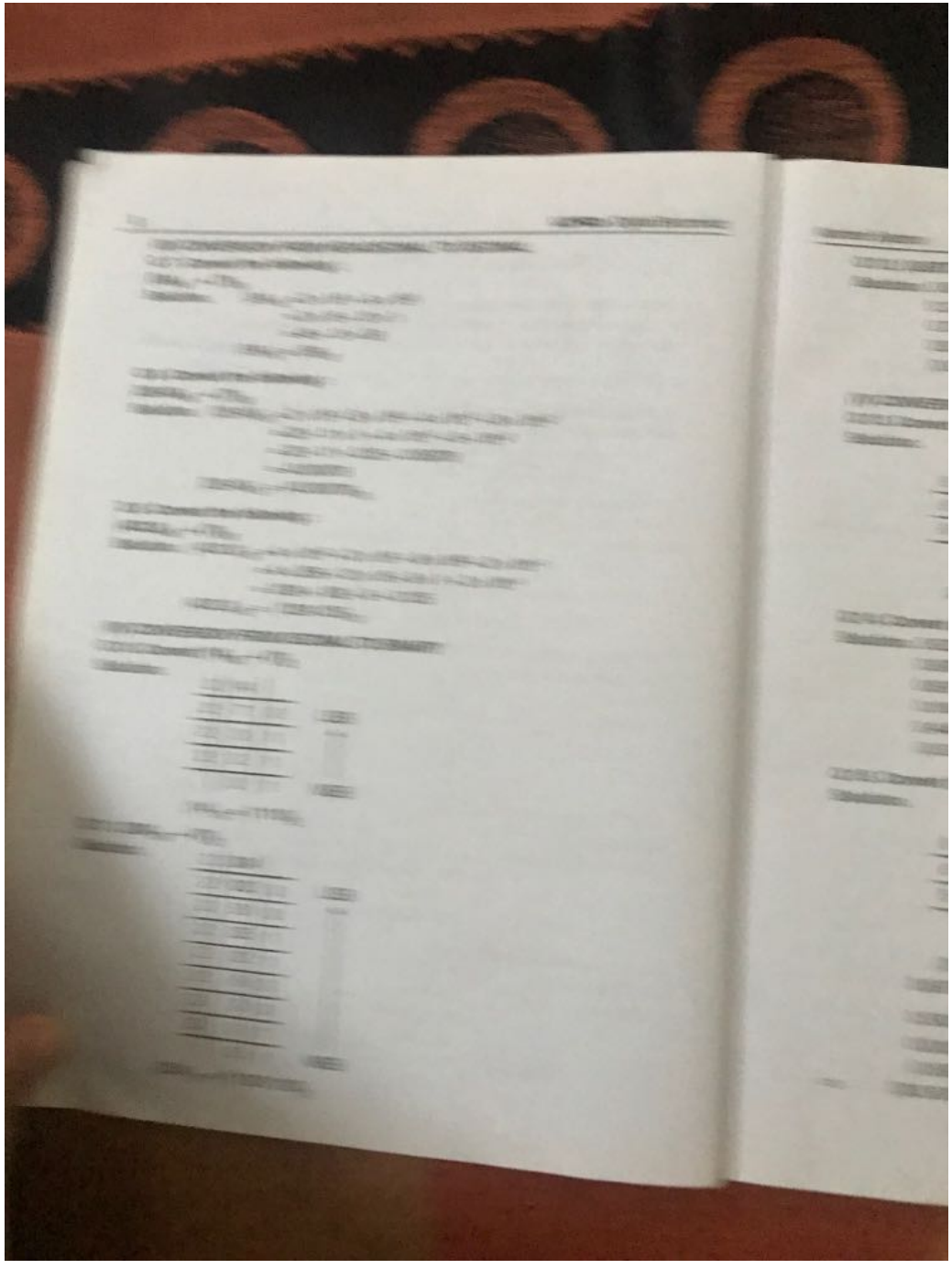
8	305		
8	38	1	LSD ↑
8	4	6	
	0	4	MSD

$(305)_{10} = (461)_8$

$0.6875 \times 8 = 5.500$	5	MSD
$0.5000 \times 8 = 4.0000$	4	↓
$0.0000 \times 0 = 0$	0	LSD

$(0.6875)_{10} = (0.54)_8$

$\Rightarrow \quad (305.6875)_{10} = (461.54)_8$



Case I : 1's complement of smaller number is :
$(11001)_2 \rightarrow (00110)_2$.

Case II : Add 1's complement to larger number :

```
   11101
  +00110
  100011
end    +1
around 00100   Final result
carry
```

Q 31. Define 1's and 2's complements. **(PTU, May 2016, 2015 ; Dec. 2007)**

Ans. 1's complement : When the given binary number is inverted once i.e. complemented once than it is known as 1's complement.

For example : Let the binary number be $(1101)_2$ so, its 1's complement is :

```
1 1 0 1
↓ ↓ ↓ ↓
0 0 1 0
```

Whole of the data is complemented once.

2's complement : When 1 is added to the 1's complement of the binary number then it is known as 2's complement.

For example : For the binary number $(1101)_2$.

```
1 1 0 1  → Given binary member
↓ ↓ ↓ ↓
0 0 1 0  → 1's complement
    + 1  → Add 1
0 0 1 1  → 2's complement
```

Q 32. (i) Convert 2222 in Hexadecimal number.
(ii) Subtract –27 from 68 using 2's complements.
(iii) Divide $(101110)_2$ by $(101)_2$. **(PTU, May 2008)**

Ans. (i) $(2222)_{10} = (?)_{16}$

16	2222	
16	138	14
	8	10

$\therefore \quad (2222)_{10} = (8AE)_{16}$

(∵ 10 = A and 14 = E in Hexadecimal)

(X) CONVERSION FROM HEXADECIMAL TO OCTAL.

Q 26. Convert $(1AF)_{16} \rightarrow (?)_8$

Solution.

$$(0001\ 1010\ 1111)_2$$

$$\underline{000}\ \underline{110}\ \underline{101}\ \underline{111} = 657$$
$$0\ \ 6\ \ 5\ \ 7$$

$$\therefore \quad (1AF)_{16} = (657)_8$$

Q 27. Convert $(3CFB.2E)_{16} = (?)_8$

Solution.

$$(0011\ 1100\ 1111\ 1011\ 0010\ 1110)_2$$

$$\underline{000}\ \underline{011}\ \underline{110}\ \underline{011}\ \underline{111}\ \underline{011}\ .\ \underline{001}\ \underline{011}\ \underline{100}$$
$$0\ \ 3\ \ 6\ \ 3\ \ 7\ \ 3\ .\ 1\ \ 3\ \ 4$$

$$(3CFB.2E)_{16} = (36373.134)_8$$

Q 28. Convert $(68.4B)_{16} = (?)_8$

Solution.

$$0110\ 1000 \cdot 0100\ 1011$$

$$\underline{001}\ \underline{101}\ \underline{000} \cdot \underline{010}\ \underline{010}\ \underline{110}$$
$$1\ \ 5\ \ 0\ .\ 2\ \ 2\ \ 6$$

$$(64.4B)_{16} = (150.226)_8$$

Q 29. Solve $(11001)_2 - (10101)_2$. **(PTU, May 2009)**

Ans.

$$\begin{array}{r} 11001 \\ -\ 10101 \\ \hline 00100 \end{array}$$

$\therefore (11001)_2 - (10101)_2 = (00100)_2$.

Q 30. Subtract $(11001)_2$ from $(11101)_2$ using 1's complement method. **(PTU, May 2009)**

Ans. $(11101)_2 - (11001)_2$ using 1's complement method is given by :

Q 20. Convert $(11010010)_2 \rightarrow (?)_8$

Solution. $11010010 = \underbrace{011}_{3}\ \underbrace{010}_{2}\ \underbrace{010}_{2}$

$\therefore \quad (11010010) = (322)_8$

Q 21. Convert $(0.1011011)_2 \rightarrow (?)_8$

Solution. $0.1011011 = 0.\ \underbrace{101}_{5}\ \underbrace{101}_{5}\ \underbrace{100}_{4}$

$\therefore \quad (0.1011011)_2 \rightarrow (0.554)_8$

(VIII) CONVERSION FROM BINARY TO HEXADECIMAL.

Q 22. Convert $(1010111)_2 \rightarrow (?)_{16}$

Solution. $1010111 = \underbrace{0101}_{5}\underbrace{0111}_{7}$

$(1010111)_2 = (57)_{16}$

Q 23. Convert $(1010\ 1111\ 1011\ 0010)_2 \rightarrow (?)_{16}$

Solution.

$$\underbrace{1010}_{A}\underbrace{1111}_{F}\underbrace{1011}_{B}\underbrace{0010}_{2}$$

$(1010\ 1111\ 1011\ 0010)_2 = (AFB2)_{16}$

Q 24. Convert $(10110110.101111001)_2 \rightarrow (?)_{16}$

Solution.

$$\underbrace{1011}_{B}\underbrace{0110}_{6}\cdot\underbrace{1011}_{B}\underbrace{1100}_{C}\underbrace{1000}_{8}$$

$(10110110.101111001)_2 = (B6.BC8)_{16}$.

(IX) CONVERSION FROM OCTAL TO HEXADECIMAL.

Q 25. Convert $(436)_8 \rightarrow (?)_{16}$

Solution.

$$\begin{array}{ccc} 4 & 3 & 6 \\ \downarrow & \downarrow & \downarrow \\ 100 & 011 & 110 \end{array}$$

$(436)_8 = (100011110)_2$

$$\underbrace{0001}_{1}\underbrace{0001}_{1}\underbrace{1110}_{D}$$

$\therefore \quad (436)_8 = (11D)_{16}$

F 3 A 7 C 2
(1111 0011 1010 0111 1100 0010)$_2$

($\because 2^n = 16$ when $n = 4 \therefore$ Pair of 4 bits are used per digit of hexadecimal)

Q 38. $(10110111)_2$ convert to octal number system. **(PTU, May 2006)**

Ans. $(10110111)_2 = (?)_8$

010 110 111
2 6 7 ($\because 2^n = 8$)

$\therefore$ $(10110111)_2 = (267)_8$ Three bits at a time can be considered for octal.

Q 39. $(736.4)_8$ convert to decimal number system. **(PTU, May 2006)**

Ans. $(736.4)_8 = (?)_{10}$

$7 \times 8^2 + 3 \times 8^1 + 6 \times 8^0 + 4 \times 8^{-1}$

$7 \times 64 + 3 \times 8 + 6 \times 1 + \frac{4}{8}$

$448 + 24 + 6 + \frac{1}{2}$

478.5

$\therefore$ $(736.4)_8 = (478.5)_{10}$.

Q 40. Perform the subtraction with the following unsigned binary number by taking the 2's complement of the subtrahend 11010 – 10000. **(PTU, Dec. 2005)**

Ans. Let A = $(11010)_2$ and B = $(10000)_2$

1's complement of B = 01111

2's complement of B = 10000

Subtract B from A, we get

Addition of A and 2's complement of B gives the result for subtraction :

$$\begin{array}{r} 1\ 1\ 0\ 1\ 0 \\ +\ 1\ 0\ 0\ 0\ 0 \\ \hline (1)\ 0\ 1\ 0\ 1\ 0 \end{array}$$

Discard Carry

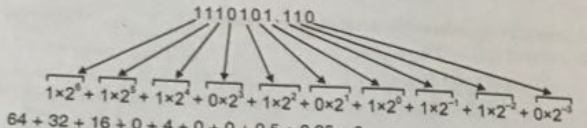
$\therefore$ 11010 – 10000 = $(01010)_2$

$(12.6875)_{10}$

$\therefore \quad (X)_{10} = (12.6875)_{10}$

Q 34. Convert the following binary numbers to decimal
(i) 1110101.110 (ii) 1101101.111

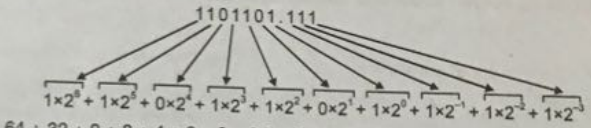
Ans. (i) N = 1110101.110 **(PTU, Dec. 2013)**



$64 + 32 + 16 + 0 + 4 + 0 + 0 + 0.5 + 0.25 + 0$

$N = (116.75)_{10} = (1110101.110)_2$

(ii) N = 1101101.111



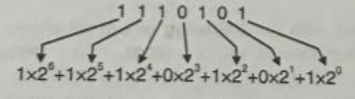
$64 + 32 + 0 + 8 + 4 + 0 + 0 + 0.5 + 0.25 + 0.125$

$N = (108.875)_{10} = (1101101.111)_2$

Q 35. Convert the following binary number in decimal 1110101.

(PTU, May 2007)

Ans. $(1110101)_2 = (?)_{10}$

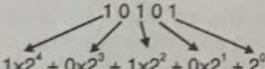


$64 + 32 + 16 + 0 + 4 + 0 + 1 \Rightarrow (117)_{10}$

$\therefore \quad (1110101)_2 = (117)_{10}$.

Q 36. Convert $(10101)_2$ to decimal number system. **(PTU, May 2018 ; Dec. 2006)**

Ans. $(10101)_2 = (?)_{10}$



$1\times2^4 + 0\times2^3 + 1\times2^2 + 0\times2^1 + 2^0\times1 \Rightarrow 16 + 0 + 4 + 0 + 1 = 21$

$\therefore \quad (10101)_2 = (21)_{10}$

Q 37. Convert hexadecimal number F3A7C2 to binary. **(PTU, Dec. 2006)**

Ans. $(F3A7C2)_{16} = (?)_2$

(ii) Subtract −27 from 68 using 2's complement

1's complement of +27

$(27)_{10} = (00011011)_2$ (for 8-bit)

1's complement ⇒ 00011011

↓↓↓↓↓↓↓↓

11100100

+ 1

2's complement 11100101

= −27

$(68)_{10} = (01000100)_2$

$$\begin{array}{r} 01000100 \\ +\ 11100101 \\ \hline \boxed{1}\ 00101001 \end{array}$$

→ Discard carry

(iii) $(101110)_2 \div (101)_2$

$$\begin{array}{r|l} 101 & 101110 \\ & 101 \\ \hline & 00110 \\ & 101 \\ \hline & 1000 \\ & 101 \\ \hline & 110 \\ & 101 \\ \hline & 1 \end{array} \quad 1001.0011$$

Q 33. Find the value of x in the following :

$(1100.1011)_2 = (x)_{10}$

Ans. **(PTU, Dec. 2007)**

$$(1100.1011)_2 = (x)_{10}$$

$$(1\times2^3 + 1\times2^2 + 0\times2^1 + 0\times2^0 + 1\times2^{-1} + 0\times2^{-2} + 1\times2^{-3} + 1\times2^{-4})_{10}$$

$$\left(8 + 4 + 0 + 0 + \frac{1}{2} + 0 + \frac{1}{8} + \frac{1}{16}\right)_{10}$$

2. Add the 1's complement to larger number

```
    11001
    01001
   ------
   100010
```

end around carry

3. Add end around carry in the result :

```
  100010
      +1   ← end around carry in added
  -------
  00011    ← Final result
```

(ii) 11011 – 11001

Using 2's complement, the steps are as follows :

1. Calculate the 2's complement of smaller number, we have

```
  11001   ← Smaller number
  00110   ← 1's complement
     +1
  -----
  00111   ← 2's complement
```

2. Add the 2's complement to larger number, we have

```
    11011
   +00111
   ------
  100010
```

Carry

3. If carry comes discard the carry, we have

Discard carry ← 100010

∴ The final result is $(00010)_2$.

Q 49. Find the value of x in the following :

(a) $(835)_{10} = (x)_{BCD}$, **(b) $(ETC.B)_{16} = (x)_8$**

(c) $(1101.101)_2 = (x)_{10}$ **(d) $(12.354)_{10} = (x)_2$**

(e) $(BEE)_x = (2699)_{10}$. **(PTU, Dec. 2007)**

Ans. (a) $(835)_{10} = (x)_{BCD}$

$= (1000\ 0011\ 0101)_{BCD}$.

(b) $(ETC.\ B)_{16} = (x)_8$

T is not possible in hexadecimal. Hence no result.

(c) $(1101.101)_2 = (x)_{10}$

$(1 \times 2^3 + 1 \times 2^2 + 0 \times 2^1 + 1 \times 2^0 + 1 \times 2^{-1} + 0 \times 2^{-2} + 1 \times 2^{-3})_{10}$

$$\left(8+4+0+1+\frac{1}{2}+0+\frac{1}{8}\right)_{10}$$

$(13.625)_{10}$

Q 46. What is a BCD code? What are its advantages and disadvantages? **(PTU, Dec. 2009 ; May 2015, 2009)**

Ans. BCD Code : BCD is the binary coded decimal code for the representation of digital data. It is a 4-bit binary number for each decimal digit.

For example : If 72 is the decimal number then its BCD code is given as :

$$(7 \quad 2)_{10}$$
$$(0111 \quad 0010)_{BCD}$$

Advantages of BCD code :

1. It make use of only 0 to 9 decimal number, thus the binary equivalent of 0 to 9 is required.
2. It is similar to the decimal number system but has 4-bit binary equivalent.

Disadvantages of BCD code :

1. BCD code needs more number of binary bits then simple binary number for representation in decimal.

For example : $(2)_{10} = (10)_2 = (0010)_{BCD}$.

2. Addition and subtraction of BCD make use of different rules.

Q 47. Convert decimal 177.25 to octal number. **(PTU, May 2017 ; Dec. 2008)**

Ans. (a) $(177.25)_{10} = (?)_8$

Integer Part

8	177	
8	22	1
	2	6

$\therefore (177)_{10} = (261)_8$

Fractional Part

$0.25 \times 8 = 2.00$

$\therefore (0.25)_{10} = (0.2)_8$

$\therefore (177.25)_{10} = (261.2)_8$

Q 48. Perform following subtraction
(i) 11001 – 10110 using 1's complement.
(ii) 11011 – 11001 using 2's complement.

Ans. (i) 11001 – 10110 **(PTU, Dec. 2008)**

Using 1's complement, the steps are :

1. Calculate the 1's complement of smaller number

10110 ← Smaller number
01001 ← 1's complement

Q 41. Write the first four decimal digits in base 4. **(PTU, Dec. 2005)**

Ans. The first four decimal digits in base 4 are :
0, 1, 2 and 3.

Q 42. Perform the subtraction with the following unsigned binary number by taking the 2's complement of the subtrahend. 1101 – 1000. **(PTU, May 2005)**

Ans. $(11010)_2 - (1000)_2$
Smaller number is $(01000)_2$
its 1's complement is $(10100)_2$
and 2's complement is $(10101)_2$
Add 2's complement of smaller number in larger number, we get :

$$\begin{array}{r} 11010 \\ +\,10101 \\ \hline \boxed{1}01111 \end{array}$$

Discard Carry

Thus, $(01111)_2$ is the final result.

Q 43. Write the first four decimal digits is base 6. **(PTU, May 2005)**

Ans. 0, 1, 2, 3 are the first four decimal digital in base 6.

Q 44. Solve $(10101)_2 - (10011)_2$. **(PTU, Dec. 2009)**

Ans. $(10101)_2 - (10011)_2$
$(10101)_2 = (21)_{10}$ ← Larger number
$(10011)_2 = (19)_{10}$ ← Smaller number

1. Calculate 2's complement of smaller number, we have

$$\begin{array}{r} 10011 \leftarrow \text{Smaller number} \\ 01100 \leftarrow \text{1's complement} \\ +\,1 \\ \hline 01101 \leftarrow \text{2's complement} \end{array}$$

2. Add the 2's complement to larger number, we have

$$\begin{array}{r} 10101 \leftarrow \text{larger number} \\ +\,01101 \\ \hline \text{Carry} \leftarrow \boxed{1}00010 \end{array}$$

3. If carry comes discard the carry, we get
$(00010)_2$ which is the final result.

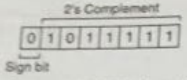
Q 45. Write the first four decimal digits in base 7. **(PTU, Dec. 2004)**

Ans. The first four decimal digits in base 7 are :
0, 1, 2, 3.

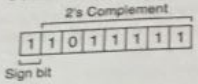
Q 52. Show the contents of an 8 bit register that stores the number + 33 and –33 in binary and sign 2's complement form. **(PTU, May 2005)**

Ans.

Contents after storing + 33 :



Contents after storing – 33 :



Q 53. Subtract $(11001)_2$ from $(11101)_2$ using 2's complement method. **(PTU, Dec. 2009)**

Ans. $(11101)_2 = (29)_{10}$ ← Larger number
$-(11001)_2 = (25)_{10}$ ← Smaller number
? Using 2's complement.

1. Calculate 2's complement of smaller number, we have

11001 ← Smaller number
00110 ← 1's complement
+ 1
00111 ← 2's complement

2. Add the 2's complement to larger number, we have

11101
+00111
Carry ← 1 00100

3. If carry comes discard it, we have
$(00100)_2$ is the final result.

Q 54. Convert binary number 1001 into gray. **(PTU, May 2010)**

Ans. $(1001)_2 = (?)_{\text{Gray code}}$

1 0 0 1
↓ ↓ ↓ ↓
$(1\ 1\ 0\ 1)_{\text{Gray Code}}$

∴ Gray code of binary $(1001)_2$ is $(1101)_{\text{Gray code}}$

Q 55. Write decimal 87 in BCD code. **(PTU, Dec. 2010)**

Ans. $(87)_{10} = (?)_{BCD}$

8 7
↓ ↓
$(1000\ \ 0111)_{BCD}$

Q 56. What is the full form of ASCII and where do we use it? **(PTU, May 2017 ; Dec. 2014, 2010)**

Ans. ASCII : American Standard Code for Information Interchange. It is used in the keyboard of computers for different alphabets, symbols etc.

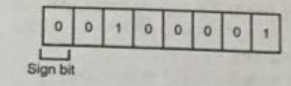
Gray Code : Gray code is mainly used in shaft position encoders. A shaft position encoder basically produces a code word which represents the angular position of the shaft.

Excess-3 code : It is non-weighted code. It is derived from 8421 BCD code. It is a sequential and self complimenting code.

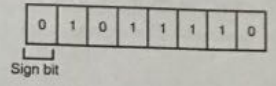
Q 51. Show that the contents of an 8 bit register that stores the number +33 in sign 1's complements and sign 2's complement form. **(PTU, Dec. 2005)**

Ans. Number N = +33

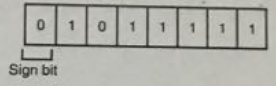
Its signed magnitude form is :



Its signed 1's complement is :

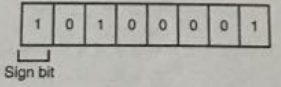


Its signed 2's complement is :

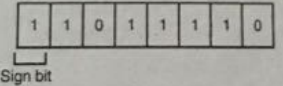


Similarly, when N = –33

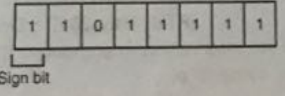
Its signed magnitude form is :



Its signed 1's complement is :



Its signed 2's complement is :



(d) $(12.354)_{10} = (x)_2$

2	12	
2	6	0
2	3	0
	1	1

LSB

MSB

$\therefore (12)_{10} = (1100)_2$

Similarly $0.354 \times 2 = 0.708$	0
$0.708 \times 2 = 1.416$	1
$0.416 \times 2 = 0.832$	0
$0.832 \times 2 = 1.664$	1
$0.664 \times 2 = 1.328$	1
$0.328 \times 2 = 0.656$	0
$0.656 \times 2 = 0.312$	0

$\therefore (12.354)_{10} = (1100.0101100 \ldots.)_2$

(e) $(BEE)_x = (2699)_{10}$

$11 \times x^2 + 14 \times x + 14 = 2699$

$11x^2 + 14x = 2685 \Rightarrow 11x^2 + 14x - 2685 = 0$

$$x = \frac{-14 \pm \sqrt{(14)^2 - 4 \times 11 \times (-2685)}}{2 \times 11}$$

$$= \frac{-14 \pm \sqrt{196 + 118140}}{22}$$

$$x = \frac{-14 \pm \sqrt{118336}}{22}$$

$$x = \frac{-14 \pm 344}{22}$$

either, $x = \frac{330}{22}$ or $x = \frac{-358}{22}$

$x = 15$ or $x =$ –ve value and is not possible

$x = 15$.

Q 50. What are ASCII codes ? What are their applications ? **(PTU, Dec. 2017)**

Ans. ASCII : American standard code for Information interchange is a 7 bit code. In binary language, only two symbols 0 and 1 are used. It is not enough to communicate using only these two symbols between two computers. Users require 26 alphabets capital and small. Numbers 0 to 9, punctuation marks and many other symbols. This all is available in ASCII code.

Now take 2's complement of binary data, we have

```
1 0 0 0 0 1 1 0 1 1   ← Given binary data
0 1 1 1 1 0 0 1 0 0   ← 1's complement
              + 1
-------------------
0 1 1 1 1 0 0 1 0 1   ← 2's complement
```

Thus, $(0111100101)_2 = (-539)_{10}$
its hexadecimal is given by

Extra zero bits are added to complete 4-bit group → 0 0 0 1 1 1 1 0 0 1 0 1

(1 E 5)$_{16}$ [$\because (E)_{16} = (1110)_2 = (14)_{10}$]

$\therefore$ 2's complement representation of $(-539)_{10}$ in hexadecimal is given by $(1E5)_{16}$

Q 63. Explain binary to gray conversion. **(PTU, Dec. 2017)**

Ans. Binary to Gray conversion is done by using following steps.

(i) Select most significant bit (MSB) and place it as it is on most significant position.
(ii) Add MSB to next bit and discard carry and place it next to MSB.
(iii) Add 2nd bit to 3rd bit and discard carry and write the result for other bits.

Example : $(1001)_2 = (?)_{\text{Gray code}}$

1 0 0 1
↓ ↓ ↓ ↓
(1 1 0 1)$_{\text{Gray Code}}$

$\therefore$ Gray code of binary $(1001)_2$ is $(1101)_{\text{Gray code}}$.

Q 64. What are the ways in which a negative number may be represented in the memory of a computer. **(PTU, Dec. 2013)**

Ans. Negative number are stored as 2's complement in memory : This is the only way by which we can store –ve numbers

But how does the CPU know if its –ve or +ve?

Let –1 can be represented in 4 bit binary as (2's comp) 1111.

15 is also represented as 1111.

So how CPU difference –1 and 15, the way to difference –1 and 15 is only the opcode which are used to do operations.

Q 65. Given that $(79)_{10} = (142)_b$ determine the value of b. **(PTU, Dec. 2012)**

Ans. $(79)_{10} = (142)_b$

$(142)_b = (b^2 \times 1 + b^1 \times 4 + b^0 \times 2)_{10} = (79)_{10}$

Thus, $b^2 + 4b + 2 = 79$

$b^2 + 4b - 77 = 0$

Q 60. Perform subtraction of 100 with 99 using 1's complement. **(PTU, Dec. 2011)**

Ans. $(100)_{10} - (99)_{10}$ using 1's complement is performed as follows :

$(100)_{10} = (1100100)_2$

$(99)_{10} = (1100011)_2$

Add $(1100100)_2$ and 1's complement of $(1100011)_2$ to perform 1's complement subtraction, we have

```
  1100100
+ 0011100   ← 1's complement of (1100011)2
 10000000
        +1
 0000001   Final result
```

End around carry

Q 61. What is the importance, applications and uses of Gray code? **(PTU, May 2019)**

Ans. Importance of gray code is that it has a very special feature as only one bit will change each time when the decimal number is incremented by '1'. Due to this reason it is also known as unit distance code.

Applications of Gray code :

1. These are used in the shaft position encoders.
2. These are used in the optical discs to produce an appropriate binary code.

Uses : Gray code is mainly used in shaft position encoders. A shaft position encoder basically produces a code word which represents the angular position of the shaft.

Q 62. What is the 2's complement representation of $(-539)_{10}$ in hexadecimal? **(PTU, Dec. 2011)**

Ans. $(-539)_{10}$ is a negative decimal number. $(+539)_{10}$ is a positive decimal number and if its 2's complement is calculated then the result is $(-539)_{10}$

2	539	
2	269	1
2	134	1
2	67	0
2	33	1
2	16	1
2	8	0
2	4	0
2	2	0
	1	0

LSB

MSB

$\therefore (539)_{10} = (1000011011)_2$

umber + 33 and –33
(PTU, May 2005)

33 :

method.
(PTU, Dec. 2009)

(PTU, May 2010)

PTU, Dec. 2010)

ec. 2014, 2010)
It is used in the

Q 57. Divide $(10101011)_2$ by $(101)_2$. (PTU, May 2011)

Ans.

```
101)10101011(10001.00101
    101
    0000101
       101
          1000
           101
           110
           101
             1
```

Q 58. If A = 1010 and B = 1001, find A – B using 2's complement method. (PTU, May 2011)

Ans. A = 1010, B = 1001

A-B using 2's complement subtraction is given by steps as follows :

(i) Calculate 2's complement of smaller number. The 2's complement of B is given by

```
  0 1 1 0
    + 1
  0 1 1 1
```

(ii) 2's complement is added to larger number

```
  0 1 1 1
  1 0 1 0   larger number
1 0 0 0 1
```

Discard carry

(iii) Carry comes discard it, we get

$(0001)_2$ as a final result.

Q 59. Prove that if A + B = A + C and A' + B = A' + C, then B = C. (PTU, Dec. 2009)

Ans.

$$A + B = A + C \quad \text{....(1)}$$

$$A' + B = A' + C \quad \text{....(2)}$$

Multiply (1) and (2), we get

$$(A + B)(A' + B) = (A + C)(A' + C)$$

$$AA' + AB + BA' + BB = AA' + AC + CA' + CC$$

$$0 + AB + BCA' + B = 0 + AC + CA' + C \quad (\because BB = B \;\&\; CC = C)$$

$$AB + B(A' + 1) = AC + C(A' + 1)$$

$$AB + B = AC + C \quad (\because A' + 1 = 1)$$

$$B(A + 1) = C(A + 1)$$

$$\therefore \quad B = C \quad (\because A + A = 1)$$

Hence proved.

$\therefore (11111000)_2 + (00010010)_2 = (00001010)_2$

$\therefore (-8)_{10} + (18)_{10} = (10)_{10}$

(v) 12 – (–19)

$(12)_{10} = (00001100)_2$

$(+19)_{10} = (00010011)_2$

11101100 ← 1's complement

$+\ 1$

$(-19)_{10} = 11101101$ ← 2's complement

00001100

+ (2's complement of 11101101) ← $(-19)_{10}$

$?$

00010010 ← 1's complement of $(-19)_{10}$

$+\ 1$

00010011 ← 2's complement of $(-19)_{10}$

Thus, we have

00001100

$+\ 00010011$

00011111 ← $(+31)_{10}$

$\therefore \quad 12 - (-19) = (+31)_{10}$.

Q 67. What is the difference between 1's and 2's complement? Which is better of the two for the representation of the negative numbers and why? (PTU, Dec. 2012)

Ans. 1's complement of a binary number is simply replacing all 0's by 1's and all 1's by 0's.

For example : 1's complement of $(10110)_2$ is

$1\ 0\ 1\ 1\ 0$

$\downarrow\ \downarrow\ \downarrow\ \downarrow\ \downarrow$

$0\ 1\ 0\ 0\ 1$ ← 1's complement

2's complement of a binary number is one increment of 1's complement.

For example : 2's complement of $(10110)_2$ is

$1\ 0\ 1\ 1\ 0$

$\downarrow\ \downarrow\ \downarrow\ \downarrow\ \downarrow$

$0\ 1\ 0\ 0\ 1$ ← 1's complement

$+\ 1$

$0\ 1\ 0\ 1\ 0$ ← 2's complement

2's complement is better for the representation of negative numbers because it allows us to perform the operation of subtraction by actually performing addition. It means that same circuit in a digital computer can be used for both addition and subtraction, thus it saves the hardware used in digital computer.

Q 68. What do you mean by weighted code? Give example. (PTU, May 2018, 2013)

Ans. Weighted codes are those codes which make use of weighted sum method i.e.

Add the larger number to it, we have

```
        0 0 0 1 0 0 0 1
Discard carry + 1 1 1 1 1 0 1 0
              ① 0 0 0 0 1 0 1 1
```

$\therefore \quad (00010001)_2 = (00000110)_2 = (00001011)_2$

$\therefore \quad (17)_{10} - (6)_{10} = (11)_{10}$

(iii) –18 – 16

```
  – 18
  – 16
  ----
   ?
  ----
```

$(+18)_{10} = (00010010)_2$

```
1 1 1 0 1 1 0 1  ← 1's complement
          + 1
-----------------
1 1 1 0 1 1 1 0  ← 2's complement
```

$(-18)_{10}$ = 1 1 1 0 1 1 1 0 ← 2's complement

$(+16)_{10} = (00010000)_2$

```
1 1 1 0 1 1 1 1  ← 1's complement
          + 1
-----------------
1 1 1 1 0 0 0 0  ← 2's complement
```

$(-16)_{10}$ = 1 1 1 1 0 0 0 0 ← 2's complement

Thus, –18 – 16 is given by :

```
        1 1 1 0 1 1 1 0
Discard carry + 1 1 1 1 0 0 0 0
              ① 1 1 0 1 1 1 1 0
```

For true value calculate 2's complement of $(11011110)_2$

$(11011110)_2$

```
0 0 1 0 0 0 0 1  ← 1's complement
          + 1
-----------------
0 0 1 0 0 0 1 0  ← 2's complement
```

Thus, true value is $(-00100010)_2$

$\therefore \quad (-18 - 16)_{10} = (-34)_{10}$

(iv) –8 + (18)

$(+8)_{10} = (00001000)_2$

```
1 1 1 1 0 1 1 1  ← 1's complement
          + 1
-----------------
1 1 1 1 1 0 0 0  ← 2's complement
```

$(-8)_{10}$ = 1 1 1 1 1 0 0 0 ← 2's complement

$(+18)_{10} = (00010010)_2$

```
        1 1 1 1 1 0 0 0
Discard carry + 0 0 0 1 0 0 1 0
              ① 0 0 0 0 1 0 1 0
```

$$b = \frac{-4 \pm \sqrt{16 - 4.1(-77)}}{2} = \frac{-4 \pm \sqrt{16 + 308}}{2} = \frac{-4 \pm \sqrt{324}}{2} = \frac{-4 \pm 18}{2}$$

$$b = \frac{-4 + 18}{2} \quad \text{or} \quad b = \frac{-4 - 18}{2}$$

$$= \frac{14}{2} = 7 \quad \text{or} \quad b = \frac{-22}{2} = -11 \text{ (Not possible)}$$

$\therefore$ $b = 7$.

Q 66. Using 2's complement notation perform the following arithmetic operations using 8 bit register (s) :

(i) 25 + (–12) (ii) 17 – 6 (iii) –18 – 16 (iv) –8 + (18) (v) 12 – (–19)

(PTU, Dec. 2013, 2012)

Ans. (i) 25 + (–12)

$(25)_{10} = (11001)_2 = (00011001)_2$ ← Larger number

$(12)_{10} = (1100)_2 = (00001100)_2$ ← Smaller number

$25 + (-12) \Rightarrow 25 - 12$

```
  00011001  ← Larger number
- 00001100  ← Smaller number
-----------
      ?
-----------
```

2's complement of smaller number $(00001100)_2$ is given by

```
  11110011  ← 1's complement
+         1
-----------
  11110100  ← 2's complement i.e. (–12)10
-----------
```

Add the larger number to it, we have

```
    00011001  ← larger number
+   11110100  ← 2's complement of smaller number
-----------
(1) 00001101
-----------
```

Discard carry

$\therefore (00011001)_2 - (00001100)_2 = (00001101)_2$

$25 + (-12) = 13.$

(ii) 17 – 6

$(17)_{10} = (10001)_2 = (00010001)_2$

$(6)_{10} = (110)_2 = (00000110)_2$

```
  00010001  ← Larger number
- 00000110  ← Smaller number
-----------
      ?
-----------
```

2's complement of smaller number $(00000110)_2$ is given by

```
  11111001  ← 1's complement
+         1
-----------
  11111010  ← 2's complement i.e. (–6)10
-----------
```

Q 77. What is the difference between digital and binary ? **(PTU, Dec. 2017)**

Ans. Digital is discrete data where as binary means two bits '0' and '1'. Digital signals make use of binary information or data or bits. Digital signal is represented by using binary bits '0' and '1' only or bit stream.

Q 78. Convert the following numbers :

(a) $(12.25)_{10} = (?)_2$ **(b)** $(10101.1101)_2 = (?)_8$ **(c)** $(125)_8 = (?)_{10}$

(d) $(34)_{16} = (?)_2$ **(e)** $(67.2)_8 = (?)_2$ **(PTU, Dec. 2016)**

Ans. (a) $(12.25)_{10} = (?)_2$

$(12)_{10} = (1100)_2$

$(0.25)_{10} = (.01)_2$

$\therefore \quad (12.25)_{10} = (1100.01)_2$

(b) $(10101.1101)_2 = (?)_8$

$010\,101 \;.\; 110\,100$

$(2 \quad 5 \;.\; 6 \quad 4)_8$

(c) $(125)_8 = (?)_{10}$

$1 \quad 2 \quad 5$

$1 \times 8^2 + 2 \times 8^1 + 5 \times 8^0 = 64 + 16 + 5 = (85)_{10}$

(d) $(34)_{16} = (?)_2$

$3 \quad 4$

$(0011\;0100)_2 = (110100)_2$

(e) $(67.2)_8 = (?)_2$

$6 \quad 7 \;.\; 2$

$(110\;111\;.\;010)_2$

Q 79. Evaluate Following :

(a) Multiply $2A8_{16}$ by $B6_{16}$

(b) Subtract 14 from 46 using 8 bit 2's complement arithmetic. **(PTU, May 2018)**

Ans. (a)

$$\begin{array}{rrrr} & 7 & 5 & \\ & 3 & 3 & \\ & 2 & A & 8 \\ \times & & B & 6 \\ \hline & F & F & 0 \\ 1 & D & 5 & 8 \times \\ \hline 1 & E & 5 & 7 & 0 \end{array}$$

$8 \times 6 = (48)_{10} = (30)_{16}$

$(10 \times 6) + 3 = (63)_{10} = (3F)_{16}$

$(11 \times 8) = (88)_{10} = (58)_{16}$

$(11 \times 10) + 5 = (115)_{10} = (75)_{16}$

$(11 \times 12) + 7 = (29)_{10} = (1D)_{16}$

$\therefore \quad (2A8)_{16} \times (B6)_{16} = (1E570)_{16}$

(b) Subtract 14 from 46 :

$(46)_{10} = (1110)_2 = (00011110)_2$ for 8-bit data

$(14)_{10} = (1110)_2 = (00001110)_2$ for 8 bit data.

Calculate 2's complement of smallest number, we get

$$\begin{array}{rr} & 00001110 \\ & 11100001 \quad \leftarrow \text{1's complement} \\ + & \quad\;\; 1 \\ \hline & 11100010 \quad \leftarrow \text{2's complement} \end{array}$$

Add above in largest number, we get

$$\begin{array}{r} 11100010 \\ 00101110 \\ \hline (1)\,00010000 \end{array}$$

Discard carry

$(00010000)_2 = (32)_{10}$

❑❑❑

the higher voltage represent a '1' and the lower voltage represent '0' from the two given voltages then the system is called a +ve logic system.

Negative Logic : If lower voltage represent '1' and higher voltage represent '0' from the given two voltages, thus the system is called a –ve logic system.

Q 72. How is a + 0 and –0 represented in 1's complement. **(PTU, Dec. 2013)**

Ans. If most significant bit i.e. the left most bit represent the sign of the number. i.e. if MSB is '1' than the number is in negative (–ve) form and if MSB is '0' then the number is in positive (+ve) form.

As $0 = 000$

is compliment of '0' is = 111

Value of '–0' is = $\boxed{1}111$

↑

Shows –ve form

Value of '+0' is = $\boxed{0}111$.

↑

Shows +ve form

Q 73. What do you mean by non-weighted code? Give example. (PTU, Dec. 2014)

Ans. In these codes it is not possible to assign weights to the binary bits or digits according to their positions i.e., each position within the binary number is not assigned a specific value or weight. Examples of non-weighted codes are : Excess-3 codes and Gray codes.

Q 74. What is the difference between BCD and Binary numbers? (PTU, Dec. 2015)

Ans.

BCD numbers	Binary numbers
(i) BCD stands for binary coded decimal code and is a four bit code for single digit.	(i) Binary number does not ristricted to four bit code. It has a binary weighted code system.
(ii) BCD of $(15)_{10}$ is $(00010101)_{BCD}$	(ii) Binary of $(15)_{10}$ is $(1111)_2$.

Q 75. What is the decimal equivalent of Binary number 11010? (PTU, May 2015)

Ans. The decimal equivalent of binary number 11010 is given by

$$(11010)_2 = 1\times2^4 + 1\times2^3 + 0\times2^2 + 1\times2^1 + 2^0\times0$$
$$= 16 + 8 + 0 + 2 + 0$$
$$= (26)_{10}$$

Q 76. Multiply 1011.01 with 110.1. **(PTU, May 2019)**

Ans. 1011.10 × 110.1 ⇒

```
    1011.01
     110.10
  ----------
    00000000
     1011.01x
    0000.00xx
   1011.01xxx
  1011.01xxxx
  ----------
  1001001.0010
```

$= (1001001.001)_2$

which obey the principle of positional weight. In weighted codes each position of the number has a specific weight

Weighted codes are :

1. Binary codes
2. BCD codes. For example : 8421, 2421, 4221, 5311, 7421, $84\overline{2}\overline{1}$ etc.

Q 69. Convert the following decimal numbers to binary
(i) 104 (ii) 1998

Ans. **(PTU, Dec. 2013)**

(i) 104

2	104	
2	52	0
2	26	0
2	13	0
2	6	1
2	3	0
2	1	1

LSB

MSB

$\therefore \quad (104)_{10} = (1101000)_2$

(ii) 1998

2	1998	
2	999	0
2	499	1
2	249	1
2	124	1
2	62	0
2	31	0
2	15	1
2	7	1
	3	1

$\therefore \quad 1998 = (1111001110)_2$

Q 70. Subtract the following binary numbers using 2's compliment
(i) 11010-1101 (ii) 10010-10011 **(PTU, Dec. 2013)**

Ans.

(i) 11010-1101

minuend = 11010
Subtrahend = 1101
2's compliment of subtrahend, 1101 is

0 0 1 0
+ 1
0 0 1 1

Now add minuend, 11010 to 0011

1 1 0 1 0
0 0 1 1
1 1 1 0 1

Hence Final result = $(11101)_2$

(ii) 10010-10011

minuend = 10010
Subtrahend = 10011
2's compliment of subtrahend 10011 is

0 1 1 0 0
+ 1
0 1 1 0 1

Now add minuend, 10010 to 01101

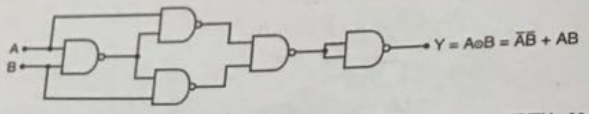
1 0 0 1 0
0 1 1 0 1
1 1 1 1 1

Hence Final result = $(1111)_2$

Q 71. What is meant by positive and negative logic? **(PTU, Dec. 2013)**

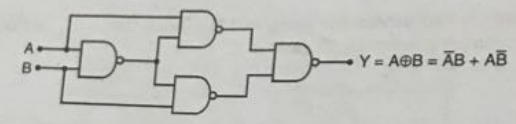
Ans. Positive Logic : As two voltage level represent the two binary digits '1' and '0'. If

(iv) XNOR gate using NAND only :



Q 5. Design EX-OR gate using NAND gates only. **(PTU, May 2011)**

Ans. EXOR gate using NAND gates only :



Q 6. What is the meaning of universal gates? **(PTU, Dec. 2011)**

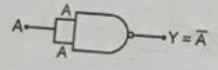
OR

Why NAND gates is called universal gate ? **(PTU, Dec. 2015)**

Ans. Universal gates are those gates from which we can design all other gates. For example NAND and NOR gates. These are called universal gates because these are used to design any gate.

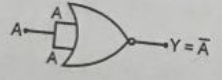
Q 7. Realize NOT gate using NAND and NOR gates separately. **(PTU, Dec. 2011)**

Ans. NOT gate using NAND gate is as shown :



$\left(\because Y = \overline{A.A} = \bar{A}\right)$

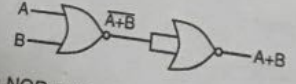
NOT gate using NOR gate is as shown :



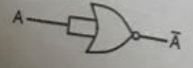
$\left(\because Y = \overline{A + A} = \bar{A}\right)$

Q 8. Realize OR and NOT using NOR gates. **(PTU, Dec. 2010 ; May 2006)**

Ans. (i) OR gate using NOR gates :



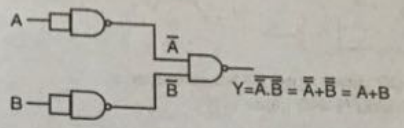
(ii) NOR gate using NOR gate only :



Q 2. Realize OR gate using NAND gates only. **(PTU, May 2007)**

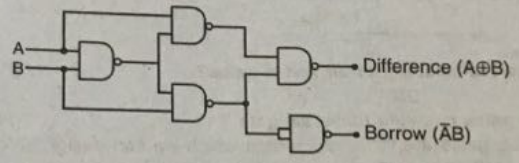
Ans. OR gate using NAND gates only :

$$Y = \overline{\overline{A}.\overline{B}} = \overline{\overline{A}} + \overline{\overline{B}} = A + B.$$



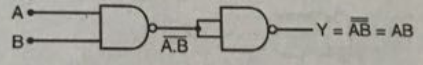
Q 3. Implement half subtractor using NAND gates. **(PTU, May 2010)**

Ans. Half subtractor using NAND gates :

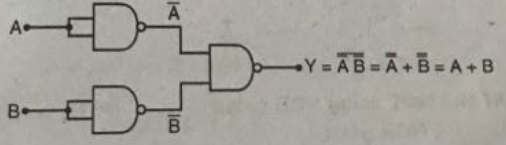


Q 4. Realize AND, OR, X-OR, X-NOR gates with the help of only NAND gates. **(PTU, Dec. 2010)**

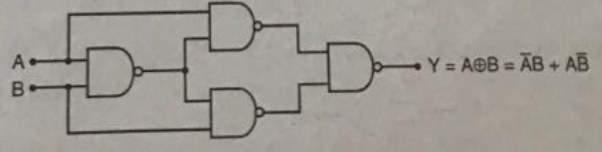
Ans. (i) AND gate using NAND Only :



(ii) OR gate using NAND only :



(iii) XOR gate using NAND only :



Chapter 2

Logic Gates

Contents

AND, OR, NOT, NAND, NOR, Exclusive-OR and Exclusive-NOR. Implementations of Logic Functions using gates, NAND-NOR implementations.

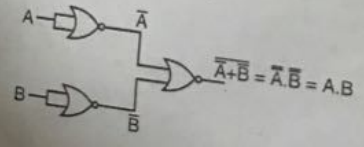
POINTS TO REMEMBER

- Logical gates most commonly used are AND, OR, NOT, NAND, NOR, XOR, XNOR.
- NAND and NOR are universal gates.
- Output of AND gate is low even if one input is low (Y = A.B) where A and B are inputs and Y is the output.
- Output of OR gate is high if any one input is high (Y = A + B).
- In NOT gate, when a high is applied as input, a low appears at output and vice versa.
- NAND gate has output high when any one of its input is low.
- The output of NOR gate is high when any input is low.
- Output of XOR gate is high if one and only one input is high.
- The output of XNOR gate is high when all inputs are high.
- NAND and NOR can be used to realize any gate.
- Propagation delay is the average transition delay time for a pulse to propagate from input to output of a switching circuit.

QUESTION-ANSWERS

Q 1. Realize AND gate using NOR gates only.

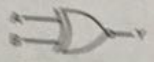
Ans. **(PTU, May 2015 ; Dec. 2016, 2007)**



Q 17. Exclusive NOR versus Exclusive OR (PTU, May 2018)

Ans. Exclusive NOR

(i) Symbol :



(ii) $Y = A \odot B = \overline{A}\overline{B} + AB$

(iii) $A \odot B = \overline{A \oplus B}$

Exclusive OR

(i) Symbol :

(ii) $Y = A \oplus B = \overline{A}B + A\overline{B}$

(iii) $A \oplus B = \overline{A \odot B}$

Q 18. Number of Gate Inputs required for expression $ABC + A\overline{B}CD + E\overline{F} + AD$. (PTU, May 2018)

Ans. $ABC + A\overline{B}CD + E\overline{F} + AD$

$= ABC + E\overline{F} + AD(\overline{B}C + 1)$

$= ABC + E\overline{F} + AD$

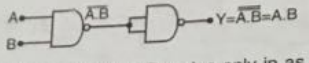
Five logic gates are required and six inputs are required.

□□□

can implement any other gate. Thus, by using NAND and NOR gates one can design or implement other gates like AND, OR, XOR, XNOR, NOT or any combination of basic gates.

Example :

(i) Implementation of AND gate using NAND gates only is as shown :



(ii) Implementation of OR gate using NOR gates only in as shown

Q 12. What is a truth table? How is it represented? What are its uses? **(PTU, Dec. 2013)**

Ans. Truth table is a mathematical table used in logic, specifically in connection with Boolean Algebra to compute the functional value of logical expressions on each of their functional arguments.

Truth-table is represented in a tabular (table) form.

Uses : In digital electronics and computer science engg., truth tables can be used to reduce basic boolean operations to simple correlation of input to outputs without the use of logic gates or code.

Q 13. How many AND gates are required to realize Y = ACD + EF + GH. **(PTU, May 2014)**

Ans. Three AND gate are required.

Q 14. Which Gate is a single input gate and why ? **(PTU, Dec. 2015)**

Ans. NOT gate is a single input gate. It has to complement the given input. Thus, if '1' is provided at the input '0' will be produced at output and vice-versa. It is used for complementing a given bit.

Q 15. Explain the NOR Gate. Specify its symbol. **(PTU, May 2017)**

Ans. NOR gate is the combination of OR and NOT gates. Its symbol is

Also, $Y = \overline{A+B}$

Q 16. Write the applications of EX-OR gate. **(PTU, May 2017)**

Ans. Applications of XOR gate

1. Arithmetic operations
2. Parity checker
3. Binary of gray code conversion
4. Gray to binary code conversion
5. Digital comparator

$A\bar{B} + AB$

TU, May 2011)

Dec. 2011)

Dec. 2015)
gates. For
are used to

Dec. 2011)

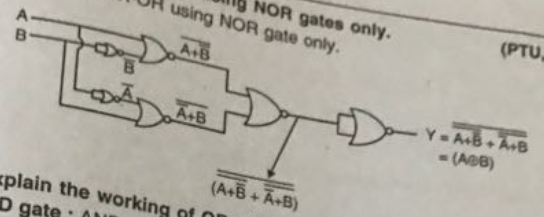
$\overline{A.A} = \overline{A}$)

$\overline{\overline{A}} = A$)

2006)

Q 9. Realize X-OR function using NOR gates only. **(PTU, Dec. 2005)**

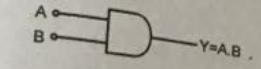
Ans. Realization of X-OR using NOR gate only.



Q 10. Explain the working of OR, AND and NOT gates. **(PTU, Dec. 2013)**

Ans. AND gate : AND gate gives logical multiplication output. The AND gate has two or more inputs and single output. The output of AND gate is low even if one input is low.

Truth table and symbol of AND gate shown below



Inputs		Output
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

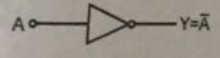
OR gate : OR gate perform logical addition. The OR gate has two or more inputs and single output. Output of OR gate is high only when any one of its input are high.

Truth table and symbol of OR gate is

Inputs		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

NOT gate : NOT gate perform the basic logical fn called inversion and complimentation. NOT gate is also called Invertor.

Truth table and symbol of NOT gate is :



Input	Output
A	Y
0	1
1	0

Q 11. Why NAND and NOR gates are called universal gate? Explain with examples. **(PTU, May 2011)**

Ans. NAND and NOR gates are called universal gates because from these gates we

2. Three Variable K-map :

'$2^n = M$' formula is used i.e. $2^3 = 8$. It means a '3' variable K-map consists of '8' squares as shown :

A \ BC	$\overline{B}\overline{C}$	$\overline{B}C$	BC	$B\overline{C}$
$\overline{A}$	$\overline{A}\overline{B}\overline{C}$	$\overline{A}\overline{B}C$	$\overline{A}BC$	$\overline{A}B\overline{C}$
A	$A\overline{B}\overline{C}$	$A\overline{B}C$	ABC	$AB\overline{C}$

OR

A \ BC	00	01	11	10
0	000	001	011	010
1	100	101	111	110

K-Map for 3-variables

Decimal Number	Variables A	B	C	Minterms Designation	Minterm	Maxterms Designation	Maxterm
0	0	0	0	$\overline{A}\overline{B}\overline{C}$	M_0	$A+B+C$	M_0
1	0	0	1	$\overline{A}BC$	M_1	$A+B+\overline{C}$	M_1
2	0	1	0	$\overline{A}B\overline{C}$	M_2	$A+\overline{B}+C$	M_2
3	0	1	1	$\overline{A}BC$	M_3	$A+\overline{B}+\overline{C}$	M_3
4	1	0	0	$A\overline{B}\overline{C}$	M_4	$\overline{A}+B+C$	M_4
5	1	0	1	$A\overline{B}C$	M_5	$\overline{A}+B+\overline{C}$	M_5
6	0	1	1	$AB\overline{C}$	M_6	$\overline{A}+\overline{B}+C$	M_6
7	1	1	1	ABC	M_7	$\overline{A}+\overline{B}+\overline{C}$	M_7

Truth Table for 3-variable K-map

3. Four Variable K-map

Formula used is $2^n = M$

Where, n = number of variables, M = Number of squares

$n = 4$

$2^4 = 16$

So, '4' variable K-map consists of '16' squares.

AB \ CD	$\overline{C}\overline{D}$	$\overline{C}D$	CD	$C\overline{D}$
$\overline{A}\overline{B}$	$\overline{A}\overline{B}\overline{C}\overline{D}$	$\overline{A}\overline{B}\overline{C}D$	$\overline{A}\overline{B}CD$	$\overline{A}\overline{B}C\overline{D}$
$\overline{A}B$	$\overline{A}B\overline{C}\overline{D}$	$\overline{A}B\overline{C}D$	$\overline{A}BCD$	$\overline{A}BC\overline{D}$
AB	$AB\overline{C}\overline{D}$	$AB\overline{C}D$	$ABCD$	$ABC\overline{D}$
$A\overline{B}$	$A\overline{B}\overline{C}\overline{D}$	$A\overline{B}\overline{C}D$	$A\overline{B}CD$	$A\overline{B}C\overline{D}$

AB \ CD	00	01	11	10
00	0	1	3	2
01	4	5	7	6
11	12	13	15	14
10	8	9	11	10

4-Variable K-map

(ii) $\overline{A.B} = \overline{A} + \overline{B}$

It states that $\overline{A} + \overline{B}$ is the complement of A . B.

Q 2. What is K-map? Why we need K-maps? Give the various types of K-map.

Ans. K-map i.e. Karnaugh map is simply a graphical method for representing a Boolean function. The Karnaugh map is a systematic method for simplify and manipulating Boolean expression. It is used to simplify a logic expression or to convert a truth table to its corresponding logic circuit. It is used for the minimization of switching functions but upto 'six' variables. For more than 'six' vairable it becomes complex or cubersome.

The K-map for n-Boolean variable switching function consists of '2^n' squares. Here each square represents the normal or standard term i.e. one minterm or maxterm.

Need of K-maps : We need K-map for representing Boolean function through graphical method. Because K-map simplify and manipulates a Boolean expression. So to solve or simplify a Boolean expression, we use K-map. K-map can be used for problems involving any number of input variables (upto six variables) which is not easily solve by Boolean Algebra.

Types of K-map : Types of K-maps commonly used are

1. Two variable K-map
2. Three variable K-map
3. Four variable K-map
4. Five variable K-map
5. Six variable K-map

1. Two variable K-map :

$2^n = M$ formula is used where, n = Number of variables and M = Number of squares.

Thus, $2^2 = 4$

∴ '2' variable K-map consists of '4' squares. It is shown in figure.

A \ B	$\overline{B}$	B
$\overline{A}$	$\overline{A}\overline{B}_{00}$	$\overline{A}B_{01}$
A	$A\overline{B}_{10}$	AB_{11}

A \ B	$\overline{B}$	B
$\overline{A}$	M_0	M_1
A	M_2	M_3

K-map for Minterms

A \ B	0	1
0	A + B	$A + \overline{B}$
1	$\overline{A} + B$	$\overline{A} + \overline{B}$

A \ B		
	M_0	M_1
	M_2	M_3

K-map for Maxterms

Truth Table for Maxterms and Minterms

Decimal Number	Variables A	Variables B	Minterm Designation	Minterm	Maxterms Designation	Maxterm
0	0	0	$\overline{A}\overline{B}$	M_0	A + B	M_0
1	0	1	$\overline{A}B$	M_1	$A + \overline{B}$	M_1
2	1	0	$A\overline{B}$	M_2	$\overline{A} + B$	M_2
3	1	1	AB	M3	$\overline{A} + \overline{B}$	M_3

Chapter

3 Boolean Algebra

Contents

Boolean postulates and laws – De-Morgan's Theorem, Principle of Duality, Boolean expression – Boolean function, Minimization of Boolean expressions – Sum of Products (SOP), Product of Sums (POS), Minterm, Maxterm, Canonical forms, Conversion between canonical forms, Karnaugh map Minimization, Don't care conditions, Quine-McCluskey method.

POINTS TO REMEMBER

- SOP involves sum of given product terms and these terms are known as minterms (m).
- POS involves product of given sum terms of these are known as maxterms (M).
- A karnaugh map is simply a graphical method for representing a boolean function. It is used to simplify a logic equation or to convert a truth table to its logic circuit.
- Types of K-map are 2 variable, 3 variable, 4 variable, 5 variable and 6 variable.
- $2^n = M$ formula is used for the calculation of total number of squares in a K-map. Here, n=number of variables and M = number of squares.
- For representing SOP form for K map; enter 1 for each minterm and 0 otherwise.
- To minimize the boolean expression using K-map, pair, Quad and octet are formed in increasing priority.
- Duality
- Q-M method in the Quine-McCluskey method or tabular method for minimization. When variables are more than six then K-map is cumber same.
- **Duality Theorem :** According to Duality theorem, from one Boolean relation other Boolean relation can be derived by
  (a) Changing each OR sign to an AND sign,
  (b) Changing each AND sign to an OR sign,
  (c) Complementing any '0' or '1' present in the expression.

QUESTION-ANSWERS

Q 1. State De-Morgans theorem. **(PTU, May 2016, 2013, 2009)**

Ans. De-Morgan's Theorem are :

(i) $\overline{A+B} = \overline{A} \cdot \overline{B}$

It states that $\overline{A} \cdot \overline{B}$ is the complement of A + B.

$\because (\overline{A}+A=1)$

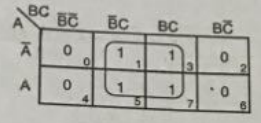
Using boolean, $Y = \overline{A}BC + \overline{A}B\overline{C}$

$= \overline{A}B(\overline{C}+C)$

$Y = \overline{A}B.1 = \overline{A}B$ $\quad \because (\overline{C}+C=1)$

$\therefore$ Minimized output of K-map is $Y = \overline{A}.B$

(ii) $F(A, B, C) = \Sigma m\ (1, 3, 5, 7)$



$Y = C$

Using boolean, $Y = \overline{A}\overline{B}C + \overline{A}BC + A\overline{B}C + ABC$

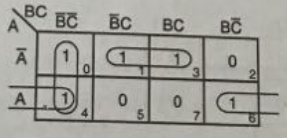
$= \overline{A}C(\overline{B}+B) + AC(\overline{B}+B)$

$= \overline{A}C.1 + AC.1$ $\quad (\because \overline{B}+B=1)$

$Y = \overline{A}C + AC = C(\overline{A}+A) = C$

$\therefore$ Minimized output of K-map is $Y = C$

(iii) $F(A, B, C) = \Sigma m\ (0, 4, 1, 3, 6)$



$Y = \overline{A}C + \overline{B}\overline{C} + AB\overline{C}$

Using boolean, $Y = \overline{A}\overline{B}\overline{C} + A\overline{B}\overline{C} + \overline{A}\overline{B}C + \overline{A}BC + AB\overline{C}$

$= (\overline{A}+A)\overline{B}\overline{C} + (\overline{B}+B)\overline{A}C + AB\overline{C}$

$= \overline{B}\overline{C}.1 + \overline{A}C.1 + AB\overline{C}$

$Y = \overline{B}\overline{C} + \overline{A}C + AB\overline{C}$

So minimized value of K-map is $Y = \overline{A}C + \overline{B}\overline{C} + AB\overline{C}$

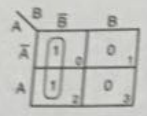
Using boolean, $Y = \overline{A}B + AB$ $\quad \because (\overline{A} + A = 1)$

$= B(\overline{A} + A)$

$= B.\ 1 = B$

So $Y = B$, is the simplified expression.

(ii) $F(A, B) = \Sigma m\ (0, 2)$



$Y = \overline{B}$

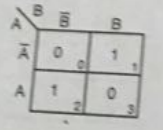
Using boolean, $Y = \overline{A}\,\overline{B} + A\overline{B}$

$= \overline{B}(\overline{A} + A)$

$= \overline{B}.1$

$\therefore\ Y = \overline{B}$

(iii) $F(A, B) = \Sigma m\ (1, 2)$



$\therefore\ Y = \overline{A}B + AB$

It is the simplified expression.

Grouping of 3 variable K-map.

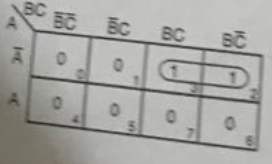
Q 4. Solve following using K-map and boolean algebra :

(i) $F(A, B, C) = \Sigma m\ (2, 3)$

(ii) $F(A, B, C) = \Sigma m\ (1, 3, 5, 7)$

(iii) $F(A, B, C) = \Sigma m\ (0, 4, 1, 3, 6)$

Solution. (i) $F(A, B, C) = \Sigma m\ (2, 3)$



$Y = \overline{A}B$

nsists of '8' squares

10
010
110

n	Maxterm
	M_0
	M_1
	M_2
	M_3
	M_4
	M_5
	M_6
	M_7

4. Five and Six Variable K-maps : Five variable K-map has $2^5 = 32$ squares and five variables are A, B, C, D and E. It is shown in figure.

BC \ DE	00	01	11	10
00	0	1	3	2
01	4	5	7	6
11	12	13	15	14
10	8	9	11	10

A = 0

BC \ DE	00	01	11	10
00	16	17	19	18
01	20	21	23	22
11	28	29	31	30
10	24	25	27	26

A = 1

Six Variable K-map i.e. (A, B, C, D, E and F) as shown :

A	CD \ EF	00	01	11	10
A = 0	00	0	1	3	2
	01	4	5	7	6
	11	12	13	15	14
	10	8	9	11	10

B = 0

CD \ EF	00	01	11	10
00	32	33	35	34
01	36	37	39	38
11	44	45	47	46
10	40	41	43	42

B = 1

A	CD \ EF	00	01	11	10
A = 1	00	16	17	19	18
	01	20	21	23	22
	11	28	29	31	30
	10	24	25	27	26

CD \ EF	00	01	11	10
00	48	49	51	50
01	52	53	55	54
11	60	61	63	62
10	56	57	59	58

Grouping of 2 variable K-map.

Q 3. Solve following using K-map and boolean algebra :

(i) F (A, B) = Σm (1, 3)

(ii) F (A, B) = Σm (0, 2)

(iii) F (A, B) = Σm (1, 2)

Solution. (i) F (A, B) = Σm (1, 3)

A \ B	$\overline{B}$	B
$\overline{A}$	0 (0)	1 (1)
A	0 (2)	1 (3)

Y = B

Q 8. Implement the function F (x, y, z) = Σ (0, 6) with NOR gates. **(PTU, Dec. 2006)**

Ans. $F(x, y, z) = \Sigma\pi (0, 6)$

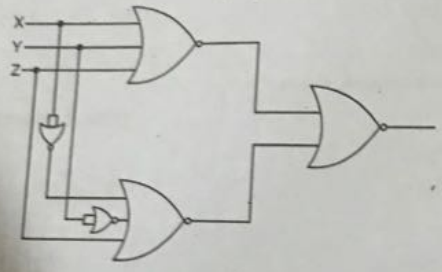
x \ yz	$\bar{y}\bar{z}$	$\bar{y}z$	yz	$y\bar{z}$
$\bar{x}$	1 (0)	0 (1)	0 (3)	0 (2)
x	0 (4)	0 (5)	0 (7)	1 (6)

$\therefore F(x, y, z) = (x + y + z)(\bar{x} + \bar{y} + z)$

By using NOR gates we have to use demorgan law :

$$\bar{\bar{F}}(x, y, z) = \overline{(x+y+z)(\bar{x}+\bar{y}+z)}$$

$$= \overline{\overline{(x+y+z)} + \overline{(\bar{x}+\bar{y}+z)}}$$



$$F(x, y, z) = \overline{\overline{(x+y+z)} + \overline{(\bar{x}+\bar{y}+z)}}$$

$$= (x + y + z)(\bar{x} + \bar{y} + z)$$

Q 9. What is don't care condition? **(PTU, Dec. 2015 ; May 2006)**

Ans. Don't Care Condition : Don't care conditions are used in K-maps. There may be cases in which the output for certain input combinations has no effect on overall output. Such conditions are known as don't care conditions. In don't care terms, output can be considered as '0' or '1' and it is designated by 'd' or 'ϕ' or 'X'. For K-map simplification 'X' can be taken as '0' or '1' so that it gives the minimized output expression.

Q 10. Convert the following logic function in a product of max terms. F (A, B, C) = (A' + B) (B' + C).

Ans. $F(A, B, C) = (A' + B)(B' + C)$ **(PTU, Dec. 2005)**

$(A' + B + CC')(B' + C + AA')$

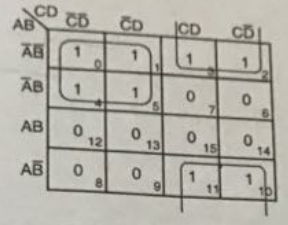
As, $A + BC = (A + B)(A + C)$

$\therefore (A' + B + CC')(B' + C + AA')$ can be written as

$F(A, B, C) = (A' + B + C)(A' + B' + C')(B' + C + A)(B' + C + A')$

(iii) F (A, B, C, D) = Σm (0, 1, 4, 5, 3, 2, 11, 10)

Solution.



$Y = \bar{A}\bar{C} + \bar{B}\bar{C}$

Using boolean, $Y = \bar{A}\bar{C} + \bar{A}\bar{B}C + A\bar{B}C$

$= \bar{A}\bar{C} + (\bar{A} + A)\bar{B}C$

$= \bar{A}\bar{C} + \bar{B}C \cdot 1$

$Y = \bar{A}\bar{C} + \bar{B}C$

Q 6. Using boolean algebraic theorems, prove that

$A + \bar{A}B + A\bar{B} = A + B$ **(PTU, Dec. 2007)**

Ans. $A + \bar{A}B + A\bar{B}$

$= A + B + A\bar{B}$ $(\because A + A\bar{B} = A + B)$

$= B + A(1 + \bar{B})$

$= B + A \cdot 1 \Rightarrow A + B$ $(\because 1 + \bar{B} = 1)$

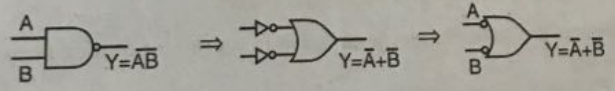
$\therefore$ L.H.S = R.H.S hence, proved.

Q 7. Define De-Morgan's theorem. **(PTU, Dec. 2012, 2009 ; May 2007)**

Ans. De Morgans Theorem :

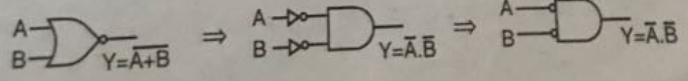
Theorem 1. It states that NAND gate can be replaced by bubbled OR gate.

i.e. $\overline{A.B.C} = \bar{A} + \bar{B} + \bar{C} + ...$



Theorem 2. It states that NOR gate can be replaced by bubbled AND gate.

i.e. $\overline{A+B+C} + ... = \bar{A}.\bar{B}.\bar{C}....$

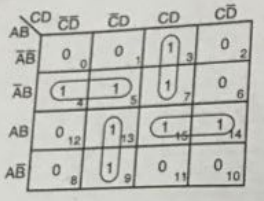


Grouping of 4 variable K-map.

Q 5. Solve the following using K-map and verify by using boolean algebra :

(i) F (A, B, C, D) = Σm (3, 4, 5, 7, 9, 13, 14, 15)

Solution.



$$Y = \bar{A}CD + \bar{A}B\bar{C} + A\bar{C}D + ABC$$

Using boolean, $Y = \bar{A}\bar{B}CD + \bar{A}B\bar{C}D + \bar{A}BC\bar{D} + \bar{A}B\bar{C}D$

$$+ AB\bar{C}D + A\bar{B}\bar{C}D + ABCD + ABC\bar{D}$$

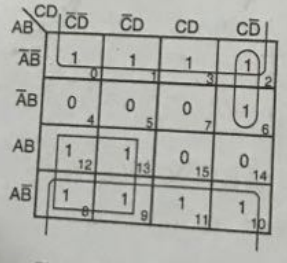
$$= \bar{A}CD(\bar{B}+B) + \bar{A}B\bar{C}(\bar{D}+D) + A\bar{C}D(B+\bar{B}) + ABC(D+\bar{D})$$

$$= \bar{A}CD.1 + \bar{A}B\bar{C}.1 + A\bar{C}D.1 + ABC.1$$

$$Y = \bar{A}CD + \bar{A}B\bar{C} + A\bar{C}D + ABC$$

(ii) F (A, B, C, D) = Σm (0, 1, 2, 3, 6, 8, 9, 10, 11, 12, 13)

Solution.



$$Y = \bar{B} + A\bar{C} + \bar{A}C\bar{D}$$

Using boolean, $Y = \bar{A}\bar{B} + A\bar{B} + \bar{A}C\bar{D} + AB\bar{C}$

$$= \bar{B}(\bar{A}+A) + \bar{A}C\bar{D} + AB\bar{C}$$

$$= \bar{B}.1 + \bar{A}C\bar{D} + AB\bar{C}$$

$$Y = \bar{B} + \bar{A}C\bar{D} + AB\bar{C}$$

$$= \bar{B} + A\bar{C} + \bar{A}C\bar{D}$$

$(\because \bar{B} + AB\bar{C} = \bar{B} + A\bar{C})$

Q 16. Write the expression for Boolean function $F(A, B, C) = \Sigma m\ (1, 4, 5, 6, 7)$ in standard POS form. **(PTU, Dec. 2008)**

Ans. $F(A, B, C) = \Sigma m\ (1, 4, 5, 6, 7)$

Standard POS form can be calculated from the following function :

$F(A, B, C) = \pi M\ (0, 2, 3)$. Because, SOP form and POS form are opposite to each other.

$\therefore$ The standard POS form expression is given by :

$$F(A, B, C) = (A + B + C)\left(A + \overline{B} + C\right)\left(A + \overline{B} + \overline{C}\right).$$

Q 17. State and prove De-Morgan's theorems.

(PTU, May 2018, 2012, 2008 ; Dec. 2017, 2013, 2011)

Ans. De-Morgan's Theorems :

(a) $\overline{A+B} = \overline{A}.\overline{B}$

It states that $\overline{A}.\overline{B}$ is the complement of A + B. Therefore, we have to prove that $(A + B) + \overline{A}.\overline{B} = 1$.

$$(A + B) + \overline{A}.\overline{B}$$

$$\Rightarrow \left[(A+B)+\overline{A}\right]\left[(A+B)+\overline{B}\right] \quad \text{(By Distributive law)}$$

$$\Rightarrow \left[\left(A+\overline{A}\right)+B\right]\left[A+\left(B+\overline{B}\right)\right] \quad \text{(By Associative law)}$$

$$\Rightarrow [1 + B]\,[1 + A]$$

$$1.1 = 1$$

$$\therefore\ (A + B) + \overline{A}.\overline{B} = 1 \qquad \text{.....(1)}$$

(b) $\overline{A.B} = \overline{A}+\overline{B}$

It states that $\overline{A}+\overline{B}$ is the complement of A.B. Therefore, we have to prove that $(A + B).\left(\overline{A}.\overline{B}\right) = 0$.

$$(A + B)\left(\overline{A}.\overline{B}\right)$$

$$\Rightarrow A\left(\overline{A}.\overline{B}\right)+B\left(\overline{A}.\overline{B}\right) \quad \text{(By Distributive law)}$$

$$\Rightarrow A.\overline{A}.\overline{B}+B.\overline{A}.\overline{B} \quad \text{(By Associative law)}$$

$$\Rightarrow 0 + 0$$

$$\Rightarrow 0$$

$$\therefore\ (A+B)\left(\overline{A}.\overline{B}\right) = 0 \qquad \text{.....(2)}$$

Q 14. Prove that if A + B = A + C and AB = AC then B = C. **(PTU, May 2009)**

Ans.
$$B = B(1 + A) \quad (\because B.1 = B \text{ and } 1 + A = 1)$$
$$= B + BA = B.B + BA \quad (\because B.B = B)$$
$$= B(B + A) = B(A + B)$$

But $A + B = A + C$ (Given)

$\therefore$ $B = B(A + C)$

$= AB + BC$

But $A.B = A.C$ (Given)

$\therefore$ $B = AC + BC$

$= C(A + B)$

But $A + B = A + C$ (Given)

$\therefore$ $B = C(A + C)$

$= AC + C.C = AC + C \quad (\because C.C = C)$

$= C(A + 1) \quad (\because A+1 = 1)$

$\therefore$ $B = C$

Hence, proved.

Q 15. Reduce the following equation using k-map

$$Y = \overline{A}\,\overline{B}\,\overline{C} + A\,\overline{C}\,\overline{D} + A\overline{B} + ABC\overline{D} + \overline{A}\,\overline{B}C. \quad \textbf{(PTU, Dec. 2008)}$$

Ans. $Y = \overline{A}\,\overline{B}\,\overline{C} + A\,\overline{C}\,\overline{D} + A\overline{B} + ABC\overline{D} + \overline{A}\,\overline{B}C$

Firstly, convert the output Y to its standard SOP form, we have

$$Y = \overline{A}\,\overline{B}\,\overline{C}(D + \overline{D}) + A(B + \overline{B})\,\overline{C}\,\overline{D} + A\overline{B}(C + \overline{C})(D + \overline{D}) + ABC\overline{D} + \overline{A}\,\overline{B}C(D + \overline{D})$$

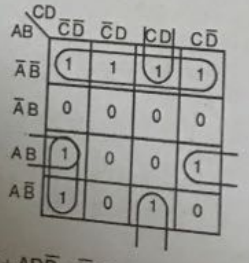
$$= \overline{A}\,\overline{B}\,\overline{C}D + \overline{A}\,\overline{B}\,\overline{C}\,\overline{D} + AB\overline{C}\,\overline{D} + A\overline{B}\,\overline{C}\,\overline{D} + (A\overline{B}C + A\overline{B}\,\overline{C})(D + \overline{D})$$

$$+ ABC\overline{D} + \overline{A}\,\overline{B}CD + \overline{A}\,\overline{B}C\overline{D}$$

$$= \overline{A}\,\overline{B}\,\overline{C}D + \overline{A}\,\overline{B}\,\overline{C}\,\overline{D} + AB\,\overline{C}\,\overline{D} + A\overline{B}\,\overline{C}\,\overline{D} + A\overline{B}CD + A\overline{B}\,\overline{C}\,\overline{D}$$

$$+ ABC\overline{D} + \overline{A}\,\overline{B}CD + \overline{A}\,\overline{B}C\overline{D}$$

$$\therefore \quad Y = \overline{A}\,\overline{B}\,\overline{C}D + \overline{A}\,\overline{B}\,\overline{C}\,\overline{D} + AB\overline{C}\,\overline{D} + A\overline{B}\,\overline{C}\,\overline{D} + A\overline{B}CD + ABC\overline{D} + \overline{A}\,\overline{B}CD + \overline{A}\,\overline{B}C\overline{D}$$



$\therefore$ $Y = \overline{A}\,\overline{B} + A\,\overline{C}\,\overline{D} + AB\overline{D} + \overline{B}CD$ is the reduced expression using k-map.

Q 11. Convert the following logic function in a product of maxterms
F (A, B, C, D) = C' D + ABC' + ABD' + A' B' D **(PTU, May 2005)**

Ans. F (A, B, C, D) = C' D + ABC' + ABD' + A' B' D

For maxterms complement the given function :

$$F(A, B, C, D) = \overline{\bar{C}D + AB\bar{C} + AB\bar{D} + \bar{A}\bar{B}D}$$

or $$\overline{\bar{C}D + AB\bar{C} + AB\bar{D} + \bar{A}\bar{B}D}$$

$$= \left(\overline{\bar{C}D}\right)\left(\overline{AB\bar{C}}\right)\left(\overline{AB\bar{D}}\right)\left(\overline{\bar{A}\bar{B}D}\right)$$

$$= \left(\bar{\bar{C}} + \bar{D}\right)\left(\bar{A} + \bar{B} + \bar{\bar{C}}\right)\left(\bar{A} + \bar{B} + \bar{\bar{D}}\right)\left(\bar{\bar{A}} + \bar{\bar{B}} + \bar{D}\right)$$

$$= (C + D)\left(\bar{A} + \bar{B} + C\right)\left(\bar{A} + \bar{B} + D\right)\left(A + B + \bar{D}\right)$$

Q 12. Convert the following logic function is a product of maxterms
F (A, B, C, D) = D (A' + B) + B'D **(PTU, Dec. 2004)**

Ans. F (A, B, C, D) = D (A' + B) + B'D
= DA' + DB + B'D

Max term can be given as :

$$\overline{DA' + DB + B'D}$$

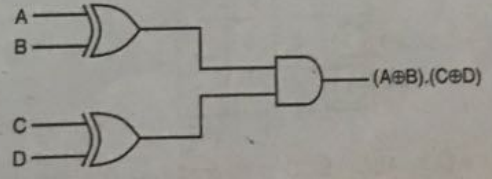
$$= \left(\overline{DA'}\right)\left(\overline{DB}\right)\left(\overline{B'D}\right)$$

$$= \left(\bar{D} + \bar{\bar{A}}\right)\left(\bar{D} + \bar{B}\right)\left(\bar{\bar{B}} + \bar{D}\right) \qquad \left(\because A' = \bar{A}\right)$$

$$F(A, B, C, D) = \left(\bar{D} + A\right)\left(\bar{D} + \bar{B}\right)\left(B + \bar{D}\right).$$

Q 13. Implement the Boolean function with exclusive -OR and AND gates :
F = AB' CD' + A' BCD' + AB' C' D + A' BC' D **(PTU, Dec. 2004)**

Ans.
F = AB' CD' + A'BCD' + AB'C'D + A'B C'D
= CD' (AB' + A'B) + C'D (AB' + A'B)
= CD' (A ⊕ B) + C'D (A ⊕ B)
= (A ⊕ B) (CD' + C'D)
= (A ⊕ B) (C ⊕ D)



(a) The Truth table from previous truth table for function F is given by

Inputs			Output
A	B	C	F
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	

(b) $F(A, B, C) = \overline{A}\,\overline{B}\,\overline{C} + \overline{A}\,\overline{B}\,C + \overline{A}B\overline{C} + \overline{A}BC + ABC$

is the expression for SOP form.

Its simplified form is given by

$$= \overline{A}\,\overline{B}\left(\overline{C}+C\right) + \overline{A}B\left(\overline{C}+C\right) + ABC$$

$$= \overline{A}\,\overline{B} + \overline{A}B + ABC \qquad \left(\because \overline{C}+C=1\right)$$

$$= \overline{A}\left(\overline{B}+B\right) + ABC$$

$$= \overline{A} + ABC$$

$$= \overline{A} + BC \qquad \left(\because \left(\overline{A}+AB\right) = \overline{A}+B\right)$$

(c) $F(A, B, C) = (A+B+C)\left(A+B+\overline{C}\right)\left(A+\overline{B}+C\right)\left(A+\overline{B}+\overline{C}\right)\left(\overline{A}+\overline{B}+\overline{C}\right)$

is the expression for POS form.

Its simplified form can be calculated from SOP form and is given as

$$\overline{A} + BC = (A)\left(\overline{B}+\overline{C}\right)$$

(d) For 2-input NAND gates, we have

$$\overline{F} = \overline{\overline{A} + BC}$$

$$F = \overline{\left(\overline{A}\right)\left(\overline{B.C}\right)}$$

$$= A.\overline{\left(\overline{B.C}\right)}$$

(A + B)

U, May 2008)

AC = $\overline{A}$ + C)

+ $\overline{A}$B = $\overline{A}$B)

($\because \overline{\overline{A}} = A$)

$= \overline{A}B + A\overline{B}$

$= A \oplus B$ = R.H.S $\quad (\because \overline{A}A = \overline{B}B = 0)$

(c) $\overline{\overline{AB} + \overline{A} + AB}$

$= \overline{\overline{A} + \overline{B} + \overline{A} + AB}$

$= \overline{\overline{A}}.\overline{B}.\overline{\overline{A}}.\overline{AB}$

$= A.B.(\overline{A} + \overline{B}) \quad (\because \overline{\overline{A}} = A)$

$= AB\overline{A} + AB\overline{B}$

$= 0$ = R.H.S. $\quad (\because A.\overline{A} = 0, B\overline{B} = 0)$

Hence proved.

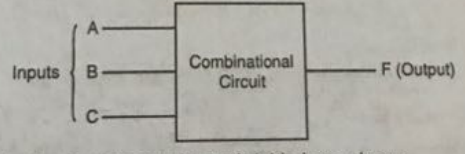
Q 19. A combinational circuit has 3 inputs A, B, C and output F. F is true for following input combinations

A is False, B is True
A is False, C is True
A, B, C are False
A, B, C are True

(a) Write the Truth Table for F. Use the convention True = 1 and False = 0.
(b) Write the simplified expression for F in SOP form.
(c) Write the simplified expression for F in POS form.
(d) Draw logic circuit using minimum number of 2 input NAND gates.

(PTU, May 2008)

Ans. The functional block diagram shows the combinational circuit :



According to thegiven inputs the truth table is as shown

A	B	C	F
0	1	X	1
0	X	1	1
0	0	0	1
1	1	1	1

(Where X = don't care as it is not given in the question for C and B inputs)

Thus, from (1) and (2) we calculated that $\overline{A}.\overline{B}$ is the complement of (A + B)

Thus, $\overline{(A+B)} = (\overline{A}.\overline{B})$

And $\overline{(A.B)} = (\overline{A}+\overline{B})$ by duality.

Q 18. Prove the following identities using Boolean algebra :

(a) $(A+B)(A+\overline{AB})+\overline{A}(B+\overline{C})+\overline{A}B+ABC = C(A+B)+\overline{A}(B+\overline{C})$

(b) $\overline{\overline{A(A.B)}.\overline{B(A.B)}} = A \oplus B.$

(c) $\overline{\overline{AB}+\overline{A}+AB} = 0.$ **(PTU, May 2008)**

Ans. (a) $(A+B)(A+\overline{AB})C+\overline{A}(B+\overline{C})+\overline{A}B+ABC$

$= (A+B)(A+\overline{A}+\overline{B})C+\overline{A}(B+\overline{C})+B(\overline{A}+AC)$

$= (A+B)(1+\overline{B})C+\overline{A}(B+\overline{C})+B(\overline{A}+C)$ $(\because \overline{A}+AC = \overline{A}+C)$

$= (A+B)C+\overline{A}(B+\overline{C})+\overline{A}B+BC$

$= AC+BC+\overline{A}B+\overline{A}\,\overline{C}+\overline{A}B+BC$

$= AC+BC+\overline{A}B+\overline{A}\,\overline{C}$ $(\because BC+BC = BC,\ \overline{A}B+\overline{A}B = \overline{A}B)$

$= C(A+B)+\overline{A}(B+\overline{C}) = R.H.S$

Hence proved.

(b) $\overline{\overline{A(\overline{A.B})}.\overline{B(\overline{A.B})}}$

$= \left[\overline{\overline{A(\overline{A.B})}}\right]+\left[\overline{\overline{B(\overline{A.B})}}\right]$

$= \left[A(\overline{A.B})\right]+\left[B(\overline{A.B})\right]$ $(\because \overline{\overline{A}} = A)$

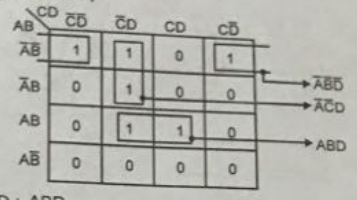
$= (\overline{A.B})(A+B)$

$= (\overline{A}+\overline{B})(A+B)$

$= \overline{A}A+\overline{A}B+\overline{B}A+\overline{B}B$

Q 22. Minimize the following expression using k-map.
$Y = \Sigma m(0, 1, 2, 5, 13, 15)$ **(PTU, May 2017)**

Ans. $Y = \Sigma m(0, 1, 2, 5, 13, 15)$



$\therefore Y = \overline{A}\overline{B}\overline{D} + \overline{A}\overline{C}D + ABD$

Q 23. Minimize the following equations using K-Map.

(a) $Y = (A + B)(A + \overline{B})(A + \overline{C})$

(b) $Y = \overline{A}B + A\overline{B}C + AB$ **(PTU, Dec. 2016)**

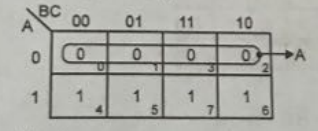
Ans. (a) $Y = (A + B)(A + \overline{B})(A + \overline{C})$

In standard form $Y = (A+B+\overline{C})(A+B+C)(A+\overline{B}+C)(A+\overline{B}+\overline{C})(A+B+\overline{C})(A+\overline{B}+\overline{C})$

$Y = (A+B+\overline{C})(A+B+C)(A+\overline{B}+C)(A+\overline{B}+\overline{C})$

$= \pi M(0, 1, 2, 3)$

K-map :



$\therefore Y = A$

(b) $Y = \overline{A}B + A\overline{B}C + AB$

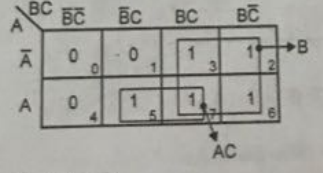
In standard form

$Y = \overline{A}B(C + \overline{C}) + A\overline{B}C + AB(C + \overline{C})$

$= \overline{A}BC + \overline{A}B\overline{C} + A\overline{B}C + ABC + AB\overline{C}$

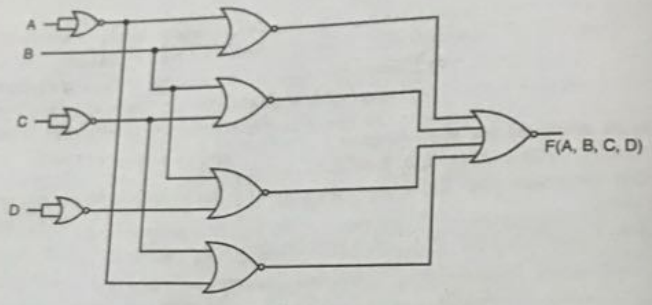
$= \Sigma m(2, 3, 5, 6, 7)$

K-map :



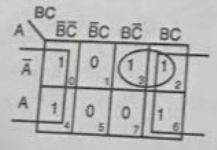
$\therefore Y = AC + B$

Logic Circuit :



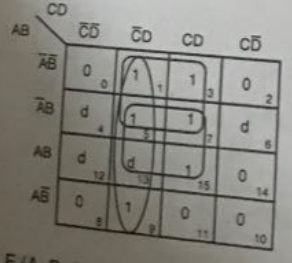
Q 21. Simplify the following boolean functions using K-maps.
(a) F (A, B, C) = Σ (0, 2, 3, 4, 6)
(b) F (A, B, C, D) = Σ (1, 3, 5, 7, 9, 15), d (A, B, C, D) = Σ (4, 6, 12, 13)
(PTU, Dec. 2007)

Ans. (a) F (A, B, C) = Σm (0, 2, 3, 4, 6)



$\therefore$ F (A, B, C) = $\bar{A}B + \bar{C}$.

(b) F (A, B, C, D) = Σm (1, 3, 5, 7, 9, 15) + Σd (4, 6, 12, 13)



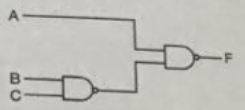
put $d_{13} = 1$
and $d_4 = d_{12} = d_6 = 0$

F (A, B, C, D) = $\bar{C}D + \bar{A}D + BD$.

$(\because \overline{C}+C=1)$

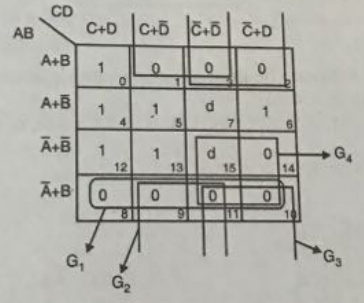
$B)=\overline{A}+B)$

Implementation using NAND gates only :



Q 20. Minimise the logic function
F (A, B, C, D) = πM (1, 2, 3, 8, 9,10, 11, 14). d (7, 15)
Use Karnaugh map. Draw the logic circuit for the simplified function using NOR gates only. **(PTU, May 2008)**

Ans. F (A, B, C, D) = πM (1, 2, 3, 8, 9,10, 11, 14). d (7, 15)



$\therefore$ F (A, B,C, D) = $G_1 . G_2 . G_3 . G_4$

Where, $G_1 = \overline{A}+B$

$G_2 = B+\overline{D}$

$G_3 = B+\overline{C}$

$G_4 = \overline{A}+\overline{C}$ ($\because$ d = 0 for 15th cell in k-map for minimization)

$\therefore$ $F(A, B, C,D) = (\overline{A}+B)(B+\overline{D})(B+\overline{C})(\overline{A}+\overline{C})$

For NOR gates implementation, we have

$$\overline{\overline{F}}(A, B, C, D) = \overline{(\overline{A}+B)(B+\overline{D})(B+\overline{C})(\overline{A}+\overline{C})}$$

$$F(A, B, C,D) = \overline{\overline{(\overline{A}+B)}+\overline{(B+\overline{D})}+\overline{(B+\overline{C})}+\overline{(\overline{A}+\overline{C})}}$$

$= \bar{A}C + \bar{A}CD + BC$

$= \bar{A}C(1 + D) + BC$

$= \bar{A}C + BC$

$= C(\bar{A} + B)$.

Q 29. Using Boolean Algebra show that

$(A + B)(\bar{A} + C)(B + C) = AC + B\bar{A}$. **(PTU, May 2010)**

Ans. $(A + B)(\bar{A} + C)(B + C)$

$= (A\bar{A} + AC + B\bar{A} + BC)(B + C)$

$= (AC + \bar{A}B + BC)(B + C)$ $(\because A\bar{A} = 0)$

$= ABC + AC.C + \bar{A}B.B + \bar{A}BC + BC.B + BC.C$

$= ABC + AC + \bar{A}B + \bar{A}BC + BC + BC$ $(\because B.B = B, C.C = C)$

$= AC(B + 1) + \bar{A}B(1 + C) + BC$ $(\because BC + BC = BC)$

$= AC + \bar{A}B + BC$

$= AC + \bar{A}B + BC(\bar{A} + A)$ $(\because A + \bar{A} = 1)$

$= AC + \bar{A}B + \bar{A}BC + ABC = \bar{A}BC(1 + C) + AC(1 + B)$

$= \bar{A}B + AC$ $(\because 1 + C = 1 + B = 1)$

$\therefore (A + B)(\bar{A} + C)(B + C) = AC + B\bar{A}$.

Q 30. Minimize the following expressions using K-map

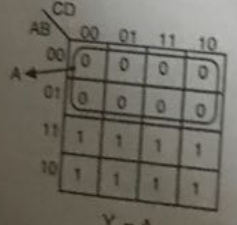
(a) $Y = (A + B)(A + \bar{B})(A + \bar{C})$

(b) $Y = \bar{A}B + A\bar{B}C + AB$

(PTU, May 2011)

Ans. (a) $Y = (A + B)(A + \bar{B})(A + \bar{C})$

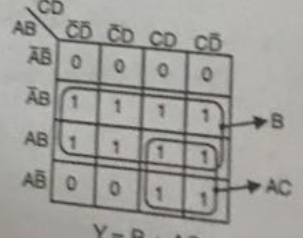
K-map :



$Y = A$

(b) $Y = \bar{A}B + A\bar{B}C + AB$

K-map :



$\therefore Y = B + AC$.

$$= AB(C+\overline{C}) + (A+\overline{A})BC + \overline{A}(B+\overline{B})(C+\overline{C})$$

$$= ABC + AB\overline{C} + ABC + \overline{A}BC + (\overline{A}B + \overline{A}\overline{B})(C+\overline{C})$$

$$\therefore \quad f = ABC + AB\overline{C} + \overline{A}BC + \overline{A}BC + \overline{A}B\overline{C} + \overline{A}\overline{B}C + \overline{A}\overline{B}\overline{C}$$

The above form is the standard SOP form.

Q 27. Construct the truth table for $Z = xy + \overline{x}\overline{y}$ (PTU, May 2011)

Ans. $Z = xy + \overline{x}\overline{y} = x \odot y$ i.e., XNOR gate.

Its truth table is

x	y	xy	$\overline{x}\overline{y}$	$xy + \overline{x}\overline{y}$
0	0	0	1	1
0	1	0	0	0
1	0	0	0	0
1	1	1	0	1

Q 28. Minimize the following expressions

(i) $A + \overline{(\overline{B} + \overline{C})}$

(ii) $\overline{(A\overline{B}(C+\overline{D}) + \overline{C})}$ (PTU, May 2011)

Ans. (i) $A + \overline{(\overline{B} + \overline{C})}$

$$= A + (\overline{\overline{B}}.\overline{\overline{C}}) \qquad \text{(DeMorgain Theorem)}$$

$$= A + BC$$

(ii) $\overline{(A\overline{B}(C+\overline{D}) + \overline{C})}$

$$= \overline{(A\overline{B}C + A\overline{B}\overline{D})}.\overline{\overline{C}}$$

$$= (\overline{A\overline{B}C})(\overline{A\overline{B}\overline{D}}).C$$

$$= (\overline{A} + B + \overline{C})(\overline{A} + B + D).C$$

$$= (\overline{A} + \overline{A}B + \overline{A}D + \overline{A}B + B + BD + \overline{A}\overline{C} + B\overline{C} + \overline{C}D)C$$

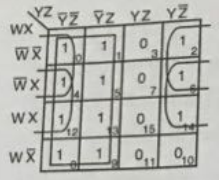
$$= \overline{A}C + \overline{A}BC + \overline{A}CD + BC + BCD + 0 + 0 + 0$$

$$= \overline{A}C(1+B) + \overline{A}CD + BC(1+D)$$

Q 24. Simplify the Boolean function : (PTU, May 2006)

$F(W, X, Y, Z) = \Sigma m\ (0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14)$

Ans.



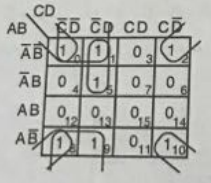
$\therefore F(W, X, Y, Z) = \overline{Y} + \overline{W}\overline{Z} + X\overline{Z}$

Q 25. Simplify the following Boolean function in :
(a) Sum of products (b) Product of sums
$F(A, B, C, D) = \Sigma\ (0, 1, 2, 5, 8, 9, 10)$. (PTU, Dec. 2006)

Ans. $F(A, B, C, D) = \Sigma\ (0, 1, 2, 5, 8, 9, 10)$

(a) Sum of products from i.e. min terms

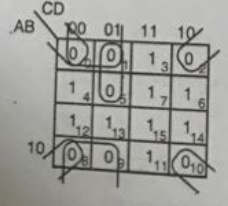
$F(A, B, C, D) = \Sigma m\ (0, 1, 2, 5, 8, 9, 10)$



$\therefore \quad F = \overline{B}\overline{C} + \overline{B}\overline{D} + \overline{A}\overline{C}D$

(b) Product of sums i.e. min terms

$F(A, B, C, D) = \Sigma M \text{ or } \pi\ (0, 1, 5, 8, 9, 10)$



$F = (B + C)\ (B + D)\ (A + C + \overline{D})$

Q 26. Find SOP form of $f = AB + BC + \overline{A}$.

Ans. $f = AB + BC + \overline{A}$ (PTU, May 2010)

Step 3 :

Pair of terms	A	B	C	D
0, 1	0	0	0	X
0, 8	X	0	0	0
1, 9	X	0	0	1
8, 9	1	0	0	X
6, 7	0	1	1	X
6, 14	X	1	1	0
9, 13	1	X	0	1
7, 15	X	1	1	1
13, 15	1	1	X	1
14, 15	1	1	1	X

Step 4 :

Quad of terms	A	B	C	D
0, 1, 8, 9	X	0	0	X
6, 7, 14, 15	X	1	1	X

Step 5 :

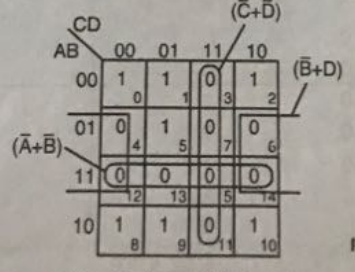
	0	1	6	7	8	9	13	14	15
* 0, 1, 8, 9	⊗	⊗			⊗	x			
* 6, 7, 14, 15			⊗	⊗				⊗	x
13, 15							x		x
9, 13						x	x		

$$F = \overline{B}\,\overline{C} + BC + ABD$$

Q 33. Obtain the minimal POS expressions for the switching function given below using a four variable K-map.

f (A, B, C, D) = π (3, 4, 6, 7, 11, 12, 13, 14, 15). **(PTU, Dec. 2010)**

Ans. f (A, B, C, D) = π (3, 4, 6, 7, 11, 12, 13, 14, 15)



$$f(A, B, C, D) = (\overline{A} + \overline{B})(\overline{C} + \overline{D})(\overline{B} + D)$$

Step 4

Quad of terms	A	B	C	D
0, 1, 8, 9	X	0	0	X
0, 8, 1, 9	X	0	0	X
6, 14, 7, 15	X	1	1	X
6, 7, 14, 15	X	1	1	X

Step 5

	0	1	3	4	6	7	8	9	14	15
0, 1, 8, 9	‡	‡					⊗	⊗		
6, 7, 14, 15					‡	‡			⊗	⊗
3, 7			‡			‡				
4, 6				‡	‡					
1, 3		‡	‡							
0, 4	‡			‡						

$$F = \overline{B}\overline{C} + BC + \overline{A}C\overline{D} + \overline{A}\overline{B}D$$

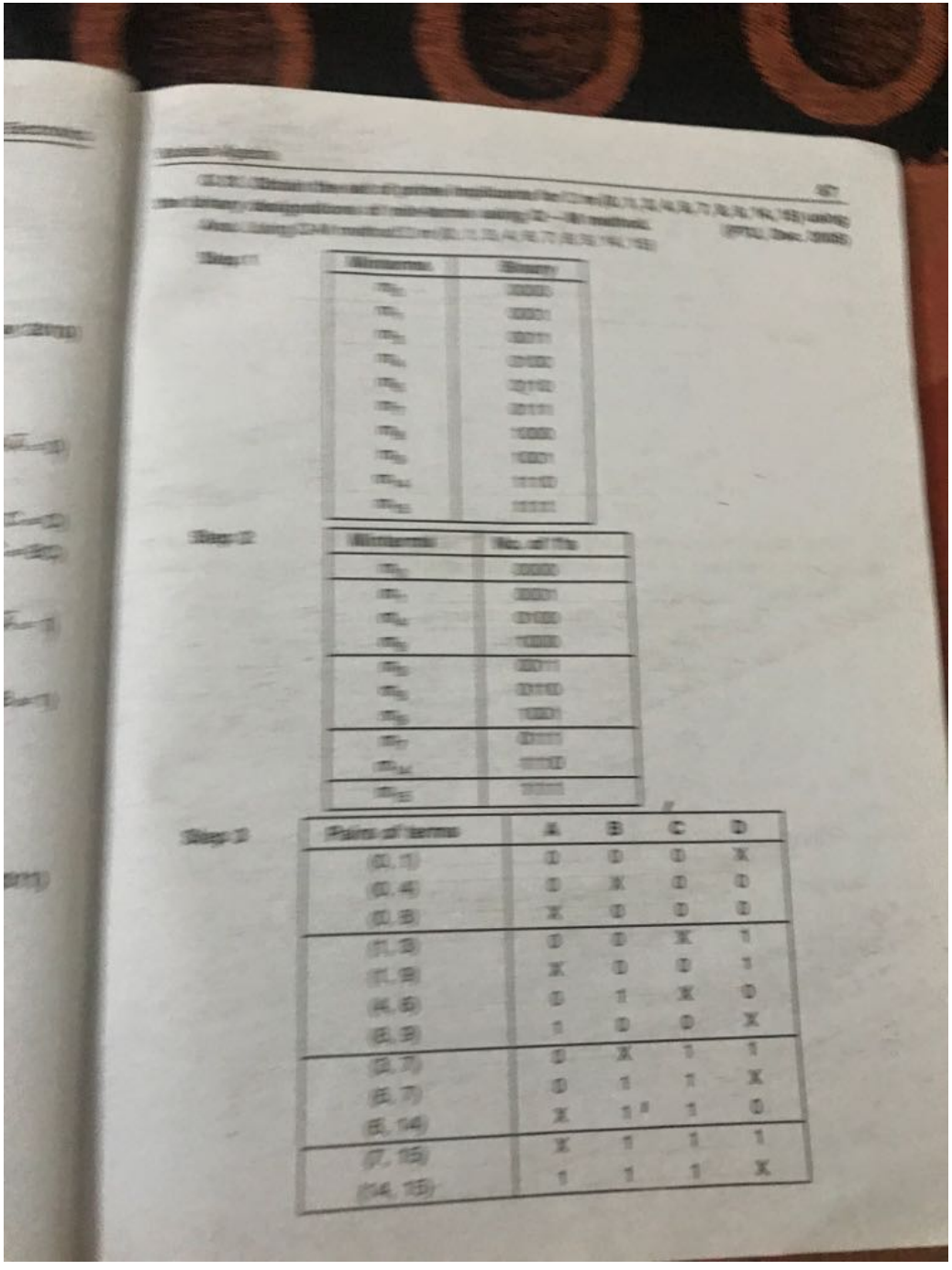
Q 32. Obtain the set of prime implicants for Σ m (0, 1, 6, 7, 8, 9, 13, 14, 15) using the binary designations of minterms using Q-M method. **(PTU, May 2005)**

Ans. Step 1 :

Minterm	Equivalent Binary
m_0	0000
m_1	0001
m_6	0110
m_7	0111
m_8	1000
m_9	1001
m_{13}	1101
m_{14}	1110
m_{15}	1111

Step 2 :

Minterm	Binary	No of 1's
0	0000	0
1	0001	1
8	1000	
6	0110	2
9	1001	
7	0111	3
13	1101	
14	1110	
15	1111	4

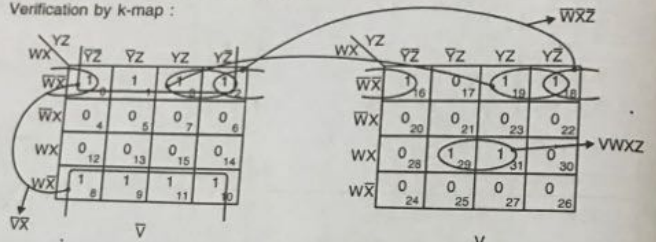


The cover 0, 2, 3, 16, 18, 19, 29 and 31 minterms.

The rest 1, 8, 9, 10, 11 are to be covered from remaining prime implicants. Thus, the minimized expression is

$$F(V, W, X, Y, Z) = VWXZ + \overline{W}\,\overline{X}\,\overline{Z} + \overline{W}\,\overline{X}Y + \overline{V}\,\overline{X}$$

Verification by k-map :



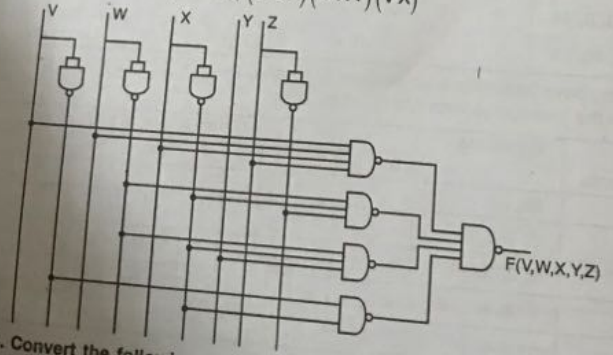
$$\therefore F(V, W, X, Y, Z) = VWXZ + \overline{W}\,\overline{X}\,\overline{Z} + \overline{W}\,\overline{X}Y + \overline{V}\,\overline{X}$$

Hence, verified.

Implementation using NAND gates only

$$\overline{F} = \overline{VWXZ + \overline{W}\,\overline{X}\,\overline{Z} + \overline{W}\,\overline{X}Y + \overline{V}\,\overline{X}}$$

$$= \overline{(VWX\overline{Z})\,(\overline{W}\,\overline{X}\,\overline{Z})\,(\overline{W}\,\overline{X}Y)\,(\overline{V}\,\overline{X})}$$



Q 35. Convert the following logic functions in a product of maxterms form.
F(A, B, C') = (A' + B) (B' + C') **(PTU, Dec. 2016)**

Ans. F (A, B, C) = (A' + B) (B' + C')

= (A' + B + C) (A' + B + C') (A + B' + C') (A' + B' + C')

F (A, B, C) = πM (3, 4, 5, 7)

Q 36. Obt
using the bina
Ans.

Minte
m
m
m
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m
m
m
m
m

Minte
m
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m
m
m
m
m
m
m
m
m

verify the result using

, 31)

Number of 1's
0
1
2
3
4
5

VXZ

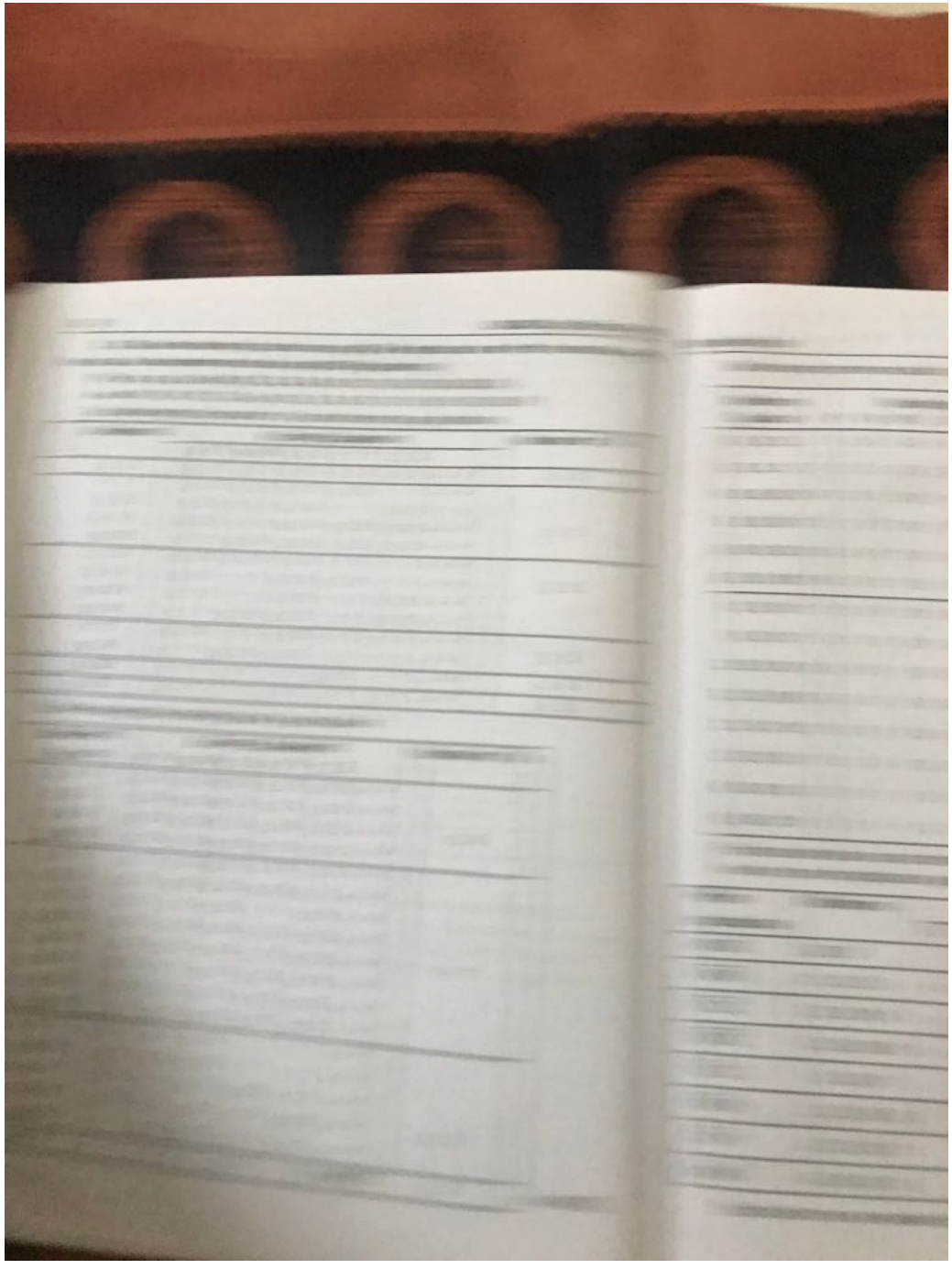
Table showing minterm quads i.e. groups of four is given below

Minterm Quads	Binary Equivalent V	W	X	Y	Z		Number of 1's	
0, 1, 2, 3	0	0	0	X	X	$\bar{V}\bar{W}\bar{X}$	0	$\Rightarrow \bar{V}\bar{W}\bar{X}$
0, 2, 1, 3	0	0	0	X	X			
0, 8, 2, 10	0	X	0	X	0	$\bar{V}\bar{X}\bar{Z}$		$\Rightarrow \bar{V}\bar{X}\bar{Z}$
0, 2, 8, 10	0	X	0	X	0			
0, 16, 2, 18	X	0	0	X	0	$\bar{W}\bar{X}\bar{Z}$		$\Rightarrow \bar{W}\bar{X}\bar{Z}$
0, 2, 16, 18	X	0	0	X	0			
1, 3, 9, 11	0	X	0	X	1	$\bar{V}\bar{X}Z$	1	$\Rightarrow \bar{V}\bar{X}Z$
1, 9, 3, 11	0	X	0	X	1			
2, 18, 3, 19	X	0	0	1	X	$\bar{W}\bar{X}Y$		$\Rightarrow \bar{W}\bar{X}Y$
2, 3, 18, 19	X	0	0	1	X			
2, 3, 10, 11	0	X	0	1	X	$\bar{V}\bar{X}Y$		$\Rightarrow \bar{V}\bar{X}Y$
2, 10, 3, 11	0	X	0	1	X			
8, 10, 9, 11	0	1	0	X	X	$\bar{V}W\bar{X}$		$\Rightarrow \bar{V}W\bar{X}$
8, 9, 10, 11	0	1	0	X	X			

From above table one octet minterm is possible i.e. 0, 1, 2, 3, 8, 9, 10, 11 $\Rightarrow \bar{V}\bar{X}$
Now the prime implicants are given by table

Prime Implicants	Minterms	Given Minterms 0	1	2	3	8	9	10	11	16	18	19	29	31
VWXZ	29, 31												⊗	⊗
$\bar{V}\bar{W}\bar{X}$	0, 1, 2, 3	×	×	×	×									
$\bar{V}\bar{X}\bar{Z}$	0, 2, 8, 10	×		×		×		×						
$\bar{W}\bar{X}\bar{Z}$	0, 2, 16, 18	×		×						⊗	×			
$\bar{V}\bar{X}Z$	1, 3, 9, 11		×		×		×		×					
$\bar{W}\bar{X}Y$	2, 3, 18, 19			×	×						×	⊗		
$\bar{V}\bar{X}Y$	2, 3, 10, 11			×	×			×	×					
$\bar{V}W\bar{X}$	8, 9, 10, 11					×	×	×	×					

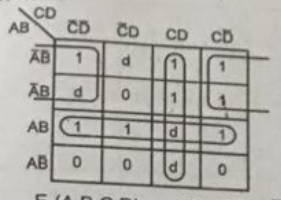
Encircle terms are essential prime implicants.



Q 37. Given F(A,B,C,D) = (0,2,3,6,7,12,13,14) +d(1,4,11,15), where d denotes the don't care condition. Find simplified expression (i) In SOP form (ii) In POS form. Also realize the simplified expression using gates. (PTU, Dec. 2015)

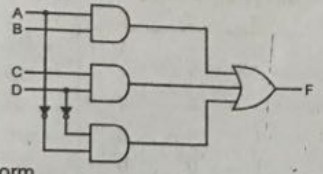
Ans. F(A, B, C, D) = Σ(0, 2, 3, 6, 7, 12, 13, 14) + d (1, 4, 11, 15)

(i) In SOP form



$F(A,B,C,D) = AB + CD + \bar{A}\bar{D}$.

Realization using gates



(ii) In POS form

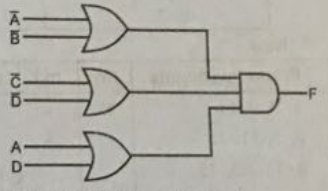
$F(A, B, C,D) = \overline{SOP} = POS$

$= \overline{AB + CD + \bar{A}\bar{D}}$

$= (\overline{AB})(\overline{CD})(\overline{\bar{A}\bar{D}})$

$= (\bar{A} + \bar{B})(\bar{C} + \bar{D})(\bar{\bar{A}} + \bar{\bar{D}})$

$= (\bar{A} + \bar{B})(\bar{C} + \bar{D})(A + D)$



Q 38. Find the minimum sum of products expression for the function f (a, b, c, d) = Σm (1, 3, 4, 6, 7, 9, 11, 12, 13, 15) using QM method. (PTU, May 2014)

Ans.

Minterms	Decimal equivalent	Binary equivalent A	B	C	D	No. of 1's used
m_1	1	0	0	0	1	1
m_3	3	0	0	1	1	2
m_4	4	0	1	0	0	1
m_6	6	0	1	1	0	2
m_7	7	0	1	1	1	3
m_9	9	1	0	0	1	2
m_{11}	11	1	0	1	1	3
m_{12}	12	1	1	0	0	2
m_{13}	13	1	1	0	1	3
m_{15}	15	1	1	1	1	4

Pair of terms	Binary Equivalent						No. of 1s
	A	B	C	D	E	F	
0, 2	0	0	0	0	–	0	0
0, 4	0	0	0	–	0	0	0
0, 8	0	0	–	0	0	0	0
0, 16	0	–	0	0	0	0	0
0, 32	–	0	0	0	0	0	0
4, 36	–	0	0	1	0	0	1
8, 24	0	–	1	0	0	0	1
8, 40	–	0	1	0	0	0	1
16, 24	0	1	–	0	0	0	1
16, 48	–	1	0	0	0	0	1
32, 36	1	0	0	–	0	0	1
32, 40	1	0	–	0	0	0	1
32, 48	1	–	0	0	0	0	1

Quad of terms	Binary Equivalent						No. of 1s
	A	B	C	D	E	F	
0, 4, 32, 36	–	0	0	–	0	0	0
0, 8, 16, 24	0	–	–	0	0	0	0
0, 8, 32, 40	–	0	–	0	0	0	0
0, 16, 8, 24	0	–	–	0	0	0	0
0, 16, 32, 48	–	–	0	0	0	0	0
0, 32, 4, 36	–	0	0	–	0	0	0
0, 32, 8, 40	–	0	–	0	0	0	0
0, 32, 16, 48	–	–	0	0	0	0	0

Prime Implicants	0	2	4	7	8	16	24	32	36	40	48
0, 4, 32, 36	×		⊗								
0, 8, 16, 24	×				×	×	⊗	×	⊗		
0, 8, 32, 40	×				×						
0, 16, 32, 48	×							×		⊗	
0, 2	×	⊗				×		×			⊗

$\therefore Y = \overline{B}\overline{C}\overline{E}\overline{F} + \overline{A}\overline{D}\overline{E}\overline{F} + \overline{B}\overline{D}\overline{E}\overline{F} + \overline{C}\overline{D}\overline{E}\overline{F} + \overline{A}\overline{B}\overline{C}\overline{D}\overline{F}$

Q 36. Obtain the set of prime implicants for Σm (0, 2, 4, 7, 8, 16, 24, 32, 36, 40, 48) using the binary designations of min terms using Q-M-method.

Ans.

Minterms	Binary Equivalent					
	A	B	C	D	E	F
m_0	0	0	0	0	0	0
m_2	0	0	0	0	1	0
m_4	0	0	0	1	0	0
m_7	0	0	0	1	1	1
m_8	0	0	1	0	0	0
m_{16}	0	1	0	0	0	0
m_{24}	0	1	1	0	0	0
m_{32}	1	0	0	0	0	0
m_{36}	1	0	0	1	0	0
m_{40}	1	0	1	0	0	0
m_{48}	1	1	0	0	0	0

Minterms	Binary Equivalent						No. of 1s
	A	B	C	D	E	F	
m_0	0	0	0	0	0	0	0
m_2	0	0	0	0	1	0	1
m_4	0	0	0	1	0	0	1
m_8	0	0	1	0	0	0	1
m_{16}	0	1	0	0	0	0	1
m_{32}	1	0	0	0	0	0	1
m_{24}	0	1	1	0	0	0	2
m_{36}	1	0	0	1	0	0	2
m_{40}	1	0	1	0	0	0	2
m_{48}	1	1	0	0	0	0	2
m_7	0	0	0	1	1	1	3

Q 43. Rewrite the following expression in a form that requires as few inversions as possible b'c + acd' + a'c + c (a + c) (a' + d'). **(PTU, Dec. 2012)**

Ans. b'c + acd' + a'c + c (a + c) (a' + d')

= b'c + c (ad' + a') + (ac + c) (a' + d') (∵ c.c = c)

= b'c + c (d' + a') + c (1 + a) (a' + d') (∵ a + a'b = a + b)

= b'c + c (a' + d') + c (a' + d') (∵ 1 + a = 1)

= b'c + c (a' + d')

= c (a' + b' + d').

Q 44. Mention all the Boolean laws and explain any two of them. **(PTU, Dec. 2014, 2012)**

OR

Expain various laws of Boolean algebra. **(PTU, Dec. 2017)**

Ans. Boolean algebra is used for analizing a logic circuit and give its mathematical operations. Various Boolean theorems are used to simplify logic circuits and logic expressions. There are various Boolean theorems or laws or rules which are given as follows :

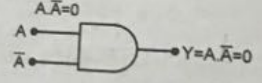
AND Laws

(a) Null Element

(b) Identity

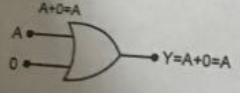
(c) Indempotent Law

(d) Complement

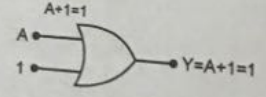


OR Laws

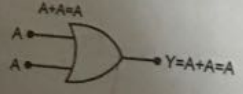
(e) Identity



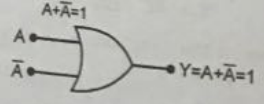
(f) Null Element



(g) Indempotent Law



(h) Complement



De-Morgan's Theorems :

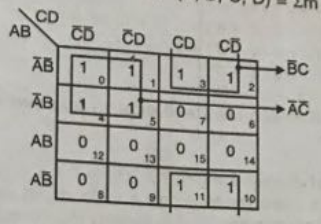
(a) $\overline{A+B} = \overline{A}.\overline{B}$

It states that $\overline{A}.\overline{B}$ is the complement of A + B. Therefore, we have to prove that

$+ B) + \overline{A}.\overline{B} = 1$

Q 40. Draw a K-map for a function of four variables F (A, B, C, D) such that F = Σm (0, 1, 4, 5, 3, 2, 11, 10) and use it to reduce this function. **(PTU, Dec. 2011)**

Ans. K-map is as shown for function F (A, B, C, D) = Σm (0, 1, 4, 5, 3, 2, 11, 10)



Therefore, the minimized or reduced function is given by

$$F(A, B, C, D) = \bar{A}\bar{C} + \bar{B}C$$

Q 41. Minimize the following boolean expression. **(PTU, May 2012)**

$$Y = \left(\bar{A}\bar{B}C + A\bar{B}\bar{C}\right)\left(\bar{A}\bar{B}C + A\bar{B}\bar{C}\right).$$

Ans.

$$Y = \left(\bar{A}\bar{B}C + A\bar{B}\bar{C}\right)\left(\bar{A}\bar{B}C + A\bar{B}\bar{C}\right)$$

$$= \left(\bar{A}\bar{B}C + A\bar{B}\bar{C}\right) \qquad (\because A.A = A)$$

$$= \left(\bar{A} + \bar{B}\right)C + A\left(\bar{B} + \bar{C}\right) \qquad \text{(Use De-Morgan's theorem)}$$

$$= \bar{A}C + \bar{B}C + A\bar{B} + A\bar{C}$$

$$= \bar{A}C + \bar{B}C + A\bar{B}\left(C + \bar{C}\right) + A\bar{C} \qquad (\because C + \bar{C} = 1$$

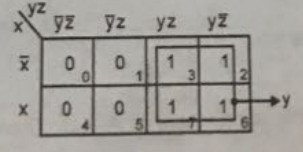
$$= \bar{A}C + \bar{B}C + A\bar{B}C + A\bar{B}\bar{C} + A\bar{C}$$

$$= \bar{A}C + \bar{B}C\left(1 + A\right) + A\bar{C}\left(\bar{B} + 1\right)$$

$$\therefore \quad Y = \bar{A}C + \bar{B}C + A\bar{C} \qquad \left(\because 1 + A = A, \bar{B} + 1 = 1\right)$$

Q 42. Represent the function (x, y, z) = y using K-map. **(PTU, Dec. 2012)**

Ans. (x, y, z) = y



∴ function (x, y, z) = y.

Minterms/ Decimal equivalent	Binary equivalent A	B	C	D	No. of 1's used
1	0	0	0	1	1
4	0	1	0	0	
3	0	0	1	1	2
6	0	1	1	0	
9	1	0	0	1	
12	1	1	0	0	
7	0	1	1	1	3
11	1	0	1	1	
13	1	1	0	1	
15	1	1	1	1	4

Prime Implicants (PI)	Binary equivalent A	B	C	D	
1, 3, 9, 11	–	0	–	1	$\rightarrow \bar{B}D$
3, 7, 11, 15	–	–	1	1	$\rightarrow CD$
9, 11, 13, 15	1	–	–	1	$\rightarrow AD$
4, 6	0	1	–	0	$\rightarrow B\bar{D}$
4, 12	–	1	0	0	$\rightarrow B\bar{C}\bar{D}$
6, 7	0	1	1	–	$\rightarrow \bar{A}BC$

Now

Prime Implicants	m1	m3	m4	m6	m7	m9	m11	m12	m13	m15
1, 3, 9, 11	⊗	×				×	×			
3, 7, 11, 15		×			×		×			×
9, 11, 13, 15						×	×		⊗	×
4, 6			×	×						
4, 12			×					⊗		
6, 7				×	×					

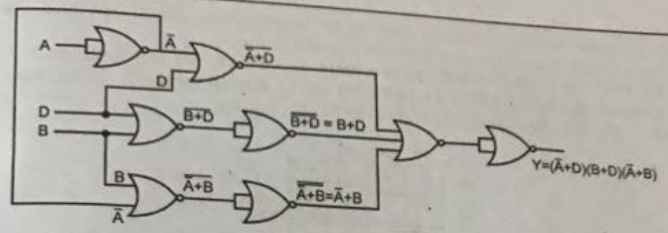
Now m_1, m_{12}, m_{13} are essential prime implicant (EPI).XO

$$Y = \bar{B}D + AD + B\bar{C}\bar{D} + \bar{A}BC$$

Q 39. Distinguish between SOP and POS forms. **(PTU, Dec. 2013)**

Ans. SOP (Sum of product) : These are expression which logically OR's the logically ANDed literals.

POS (Product of sum) : These are expression which logically AND's the logically OR'ed literals.



Q 49. State Duality Theorem. **(PTU, May 2018, 2016 ; Dec. 2014)**

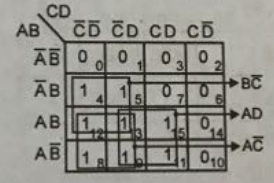
Ans. Duality Theorem : According to Duality theorem, from one Boolean relation other Boolean relation can be derived by

(a) Changing each OR sign to an AND sign,
(b) Changing each AND sign to an OR sign,
(c) Complementing any '0' or '1' present in the expression.

Q 50. Minimize the following expression using K-map. **(PTU, May 2015)**

$Y = \Sigma m(4,5,8,9,11,12,13,15)$

Ans. $Y = \Sigma m\ (4, 5, 8, 9, 11, 12, 13, 15)$

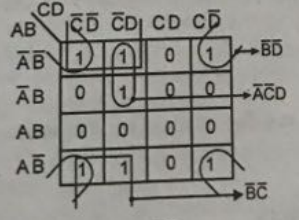


$\therefore \quad Y = B\bar{C} + A\bar{C} + AD$

Q 51. Simplify the following using K-maps :

$F(A,B,C,D) = \Sigma\ (0,1,2,5,8,9,10)$ **(PTU, Dec. 2015)**

Ans. $F(A, B,C,D) = \Sigma(0, 1, 2, 5, 8, 9, 10)$



$\therefore F(A,B,C,D) = \bar{B}\bar{C} + \bar{B}\bar{D} + \bar{A}\bar{C}D$

Q 52. What is the difference between k-map and Qm method ? (PTU, Dec. 2014)

Ans. K-map is simply a graphical method for representing a Boolean function. It is used to simplify a logic equation or to convert a truth table to its logic circuit. Q-M method is the

The essential prime implicants are :

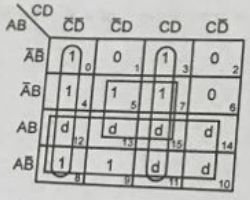
$\bar{w}x\bar{y} + w\bar{x}\bar{y} + wxy + yz$

Three distinct minimal expressions for T are :

1. $T(w, x, y, z) = \bar{w}x\bar{y} + w\bar{x}\bar{y} + wxy + yz + \bar{w}z$
2. $T(w, x, y, z) = (w + \bar{x} + y)(\bar{w} + x + y)(\bar{w} + \bar{x} + \bar{y})(\bar{y} + \bar{z})(w + \bar{z})$
3. $T(w, x, y, z) = \pi M(0, 2, 6, 10, 12, 13)$

Q 46. Simplify the following expression using K-map :
$f(A, B, C, D) = \Sigma m(0, 3, 4, 5, 7, 8, 9) + d(10, 11, 12, 13, 14, 15)$. (PTU, May 2013)

Ans. $f(A, B, C, D) = \Sigma m(0, 3, 4, 5, 7, 8, 9) + d(10, 11, 12, 13, 14, 15)$



$\therefore \quad f(A, B, C, D) = A + \bar{C}\bar{D} + CD + BD$

Q 47. Show that (A+B) (A+C) = A+BC. **(PTU, Dec. 2013)**

Ans.

L.H.S = (A+B) (A+C)
= AA + AC + BA + BC
= A + AC + AB + BC
= A (1+C) + AB + BC
= A + AB + BC
= A (1+B) + BC
= A + BC = R.H.S.

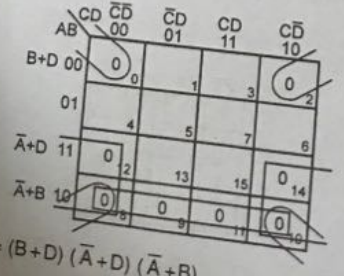
($\because$ AA = A)

($\because$ 1+C=1)

($\because$ 1+B=1)

Q 48. Simplify the expression
$F(A, B, C, D) = \Sigma(0,2,8,9,10,11,12,14)$ Using k-map in POS form and represent the resulting function using NOR gates. **(PTU, Dec. 2013)**

Ans.



$Y = (B+D)(\bar{A}+D)(\bar{A}+B)$

$(A + B) + \overline{A} . \overline{B}$

$\Rightarrow \left[(A+B)+\overline{A}\right]\left[(A+B)+\overline{B}\right]$ (By Distributive law)

$\Rightarrow \left[\left(A+\overline{A}\right)+B\right]\left[A+\left(B+\overline{B}\right)\right]$ (By Associative law)

$\Rightarrow [1 + B] [1 + A]$

$1.1 = 1$

$\therefore \quad (A + B) + \overline{A} . \overline{B} = 1$ .....(1)

(b) $\overline{A.B} = \overline{A} + \overline{B}$

It states that $\overline{A} + \overline{B}$ is the complement of A.B. Therefore, we have to prove that $(A + B).\left(\overline{A}.\overline{B}\right) = 0$.

$(A + B) \left(\overline{A}.\overline{B}\right)$

$\Rightarrow A \left(\overline{A} . \overline{B}\right) + B \left(\overline{A}. \overline{B}\right)$ (By Distributive law)

$\Rightarrow A. \overline{A}.\overline{B} + B.\overline{A}.\overline{B}$ (By Associative law)

$\Rightarrow 0 + 0$

$\Rightarrow 0$

$\therefore \quad (A+B)\left(\overline{A} . \overline{B}\right) = 0$ .....(2)

Thus, from (1) and (2) we calculated that $\overline{A} . \overline{B}$ is the complement of (A + B)

Thus, $\left(\overline{A+B}\right) = \left(\overline{A} . \overline{B}\right)$

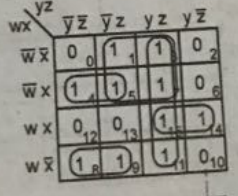
And $\left(\overline{A.B}\right) = \left(\overline{A} + \overline{B}\right)$ by duality.

Q 45. Given the function T (w, x, y, z) = Σ (1, 3, 4, 5, 7, 8, 9, 11, 14, 15)

(a) Use the K-map to determine the set of all prime implicants. Indicate specifically the essential ones. Find three distinct minimal expressions for T.

(b) Assume that only umprimed variables are available. Construct a circuit which realizes T. **(PTU, Dec. 2012)**

Ans. (a) T (w, x, y, z) = Σm (1, 3, 4, 5, 7, 8, 9, 11, 14, 15)



$T (w, x, y, z) = \overline{w}\,x\,\overline{y} + w\,\overline{x}\,\overline{y} + wxy + yz + \overline{w}z$ (or)

$= \overline{w}\,x\,\overline{y} + w\,\overline{x}\,\overline{y} + wxy + yz + \overline{x}z$

3. This helps in searching the binary minterms which are differ in one place only.
4. After separation, each binary number is compared with every term in the next higher category.
5. If they differ by only one position, a check mark is placed beside each of the two terms otherwise neglect that term and go for another term having difference of only one position.
6. Write the term in the second column with a " _ " in the position that they differed.
7. This process of comparison continuous for every minterm until, it completes.
8. Once this process is completed the same process is applied to the new resultant terms which are placed in the third column.
9. It continuous until no further elimination of literals occurs.
10. The remaining terms and all the terms that did not match during the process are called the "prime-implicants".
11. Select the minimum number of prime-implicants which must cover all the minterms.
12. Sum those prime-implicants to get the 'minimized' expression.

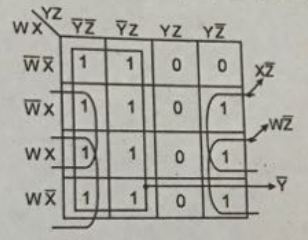
□□□

$$= AB + \bar{A}C + ABC + \bar{A}BC$$
$$= AB(1+C) + \bar{A}C(1+B)$$
$$= AB + \bar{A}C$$

(b) $AB + \bar{A}C = (A+C)(\bar{A}+B)$
$$= A\bar{A} + AB + \bar{A}C + BC$$
$$= 0 + AB + \bar{A}C + BC$$
$$= AB + \bar{A}C + BC(A+\bar{A})$$
$$= AB + \bar{A}C + ABC + \bar{A}BC$$
$$= AB(1+C) + \bar{A}C(1+B)$$
$$= AB + \bar{A}C$$

Q 57. Solve the following Boolean functions by using K-map.
$F = (W, X, Y, Z) = \sum (0, 1, 4, 5, 6, 8, 9, 10, 12, 13, 14)$ **(PTU, May 2019)**

Ans. $F(W, X, Y, Z) = \sum_m (0, 1, 4, 5, 6, 8, 9, 10, 12, 13, 14)$



$$\therefore \quad F = \bar{Y} + X\bar{Z} + W\bar{Z}$$

Q 58. Give the introduction of Quine-McCluskey method of minimization.
(PTU, May 2019)

Ans. QM method or Quine Mc-Cluskey method or Tabular Method

In case the number of variables increases i.e. 7, 8, 9 or even 10 variables. It is difficult to use K-map as it becomes very complex and the grouping techniques becomes cumbersome. So, K-map can be used for 5 or 6 variables only. Mapping methods fails for large number of variables. To overcome this problem W.V Quine and E.J. Mc-Cluskey developed a tabular method also known as QM method (i.e. Quice Mc-Cluskey Method) which is used for minimization of large number of variable.

It make use of same techniques as of K-map but in this minterms are written in the binary form first and the binary equivalents which are differ only in the place can be combined for reduction of minterms.

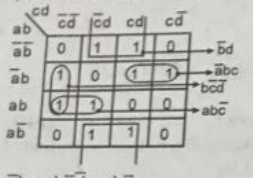
Following points are followed for Q-M Method minimization :

1. Write the given minterms in their binary form.
2. Group the minterms according to number of 1's contained in them and separate by a horizontal line between each number of 1's category. Put them in a table having separate columns.

Quine-Mc Cluskey method or tabular method for minimization. When variables are more than six then K-map is cumbersome and Qm method is used.

Q 53. Find the minimum sum of products expression for the function.
$f(a,b,c,d) = \Sigma m(1,3,4,6,7,9,11,12,13,15)$ using K-map method. (PTU, May 2016)

Ans. $f(a, b, c, d) = \Sigma m\ (1, 3, 4, 6, 7, 9, 11, 12, 13, 15)$

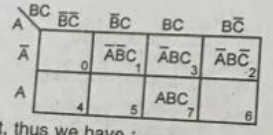


$f(a, b, c, d) = \bar{b}d + \bar{a}bc + bc\bar{d} + ab\bar{c}$

Q 54. Explain the K-map reduction technique. (PTU, May 2017)

Ans. K-map reduction technique is one of the minimized technique used for minimization. K-map reduction technique make use of one bit change in adjacent cells so that grouping takes place and minimization will be done easily.

Example : Three variable K-map :



Cell 1 and 3 are adjacent, thus we have :

$\bar{A}\bar{B}C + \bar{A}BC \Rightarrow \bar{A}C(\bar{B} + B) \Rightarrow \bar{A}C$ variable. Thus one variable is eliminated.

Similarly, cell 3 and 7 are adjacent. Thus, we have

$\bar{A}BC + ABC \Rightarrow BC\,(\bar{A} + A) \Rightarrow BC.$

Thus, one variable is eliminated. In this way K-map is used as a reduction technique.

Q 55. What are Min and Max terms ? (PTU, Dec. 2017)

Ans. Each fundamental product in the SOP form is called as minterm. These are designated by 'm'.

Example : $Y = \underbrace{\bar{A}B}_{\text{minterm}} + \underbrace{A\bar{B}C}_{\text{minterm}}$

Each fundamental sum in the POS form in called as maxterm. These are designated by 'M'.

Example : $Y = \underbrace{(A+\bar{B})}_{\text{maxterm}}\ \underbrace{(\bar{A}+B+\bar{C})}_{\text{maxterm}}$

Q 56. Using Boolean algebra show that

(a) $AB + \bar{A}C + BC = AB + \bar{A}C$

(b) $AB + \bar{A}C = (A + C)(\bar{A} + B)$

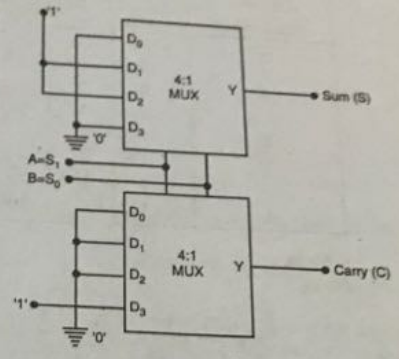
Ans. (a) $AB + \bar{A}C + BC(A + \bar{A})$

(PTU, May 2018)

Q 5. Implement half adder circuit using 4 : 1 MUX or multiplexers only.

Ans. Truth table of half adder is as shown :

Inputs		Outputs	
A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1



Q 6. Implement using 4 : 1 MUX

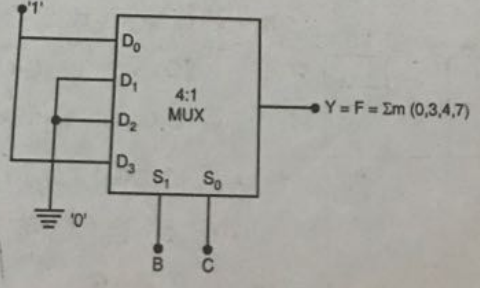
$$F = \Sigma m (0, 3, 4, 7)$$

Ans. The implementation table is as shown :

	D_0	D_1	D_2	D_3
$\overline{A}$	(0)	1	2	(3)
A	(4)	5	6	(7)

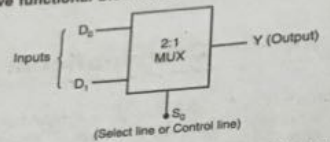
[1 0 0 1] Inputs to Multiplexer

Implementation :



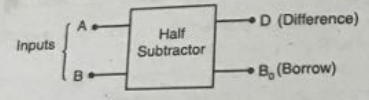
Q 2. Give functional block diagram of 2 : 1 MUX.

Ans.



Q 3. Explain half subtractor with the help of its internal circuit.

Ans. To subtract two numbers i.e. two input variables A and B, we get two output variables i.e. difference 'D' and borrow 'B_0'. It is known as half subtractor. Functional diagram is as shown :



Its truth table is as shown :

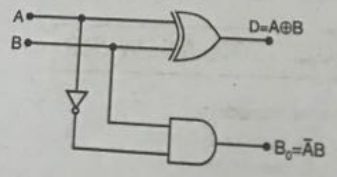
Inputs		Outputs	
A	B	D	B_0
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Thus, the minimized logic functions are :

$$D = \bar{A}B + A\bar{B} = A \oplus B$$

$$B_0 = \bar{A}B$$

The circuit diagram is as shown :



Q 4. How many full adders are required to construct an m-bit parallel adders? **(PTU, Dec. 2011)**

Ans. To construct an m-bit parallel adder, 'm' full address are required.

Chapter 4

Combinational Circuits

Contents

Design procedure – Adders, Subtractors, BCD adder, Magnitude Comparator, Multiplexer/ Demultiplexer, encoder/decoder, parity checker, code converters. Implementation of combinational logic using MUX, BCD to 7 segment decoder.

POINTS TO REMEMBER

- Combinational circuits are adders, subtractors, multiplexers, demultiplexer, magnitude comparator, parity generator/checker etc.
- Arithmetic circuits are used for addition, subtraction, multiplication, division.
- Half adder is used for addition of two binary numbers.
- Full adder is used to perform addition of more than 2 bits.
- Serial adder require one full adder for one additional bit while parallel adders requires N-full adders for n bit addition.
- Two more adders are look ahead carry adder and BCD adder.
- Half subtractor subtracts two numbers we get two output variables i.e. difference and borrow.
- Full adder is subtraction of 3 bits.
- Encoder converts human language into machine language.
- Decoder is used to convert machine language to human language.
- Multiplexers are universal circuits which selects one input out of multiple inputs and give it as a result. These are abbriviated as MUX.
- Demultiplexer receives information on single line and distribute to the 2^n lines, where n are selection lines. These are abbriviated as DEMUX.
- Magnitude comparator is used to compare 2 binary numbers.

QUESTION-ANSWERS

Q 1. List the applications of decoders.

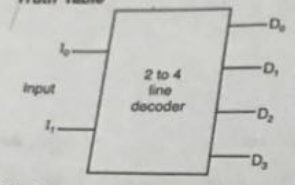
Ans. 1. Decoders are used in counter systems.
2. Decoders are uesd for A/D conversion.
3. Decoders are used for D/A conversion.
4. Decoders are used in seven segment digital displays.

into 'n' bit binary word. It is such that one of the output line will be activated for one of the possible input combinations. Demultipluters are also known as decoders.

For example : 2 to 4 line decoder is as shown ;

It has 2 inputs and 4 outputs.

Truth Table



I_0	I_1	D_0	D_1	D_2	D_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

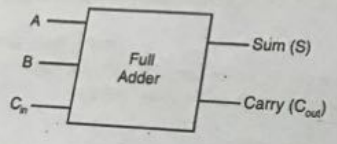
Q 12. Explain the working of full adder with example.

(PTU, Dec. 2017 ; May 2017, 2006)

OR

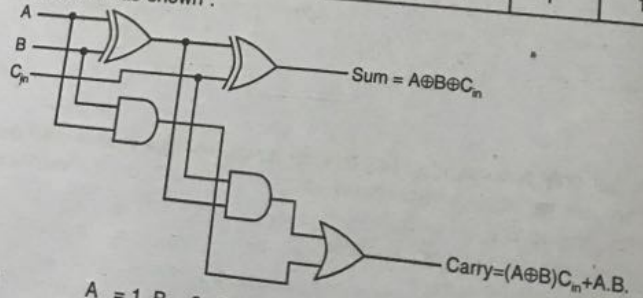
Design full adder using logic gates. **(PTU, May 2011)**

Ans. Full adder is a combinational circuit capable of adding three bits at a time (i.e. two input bits and one previous carry). Full adder has three inputs and two outputs as shown in diagram.



A	B	C_{in}	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Internal Structure in as shown :



Example :

A = 1, B = 0, C_{in} = 0

Sum = A ⊕ B ⊕ C_{in} = 1

Carry = (A ⊕ B) C_{in} + AB = 0.

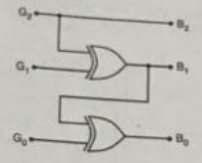
er.
conversion is as shown :

Binary Code		
B_2	B_1	B_0
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

$\overline{G_0} + G_1 G_0)$

$)$

Circuit implementation is as shown :



Q 8. List two applications of De-Multiplexer.

Ans. Two applications of De-Multiplexer are : **(PTU, May 2009)**

(i) Demultiplexer can be used to implement few combinational circuits such as full-subtractor, full-adder etc.

(ii) Demultiplexer is used in time division multiplexing at the receving end.

Q 9. What does the term driver mean in a decoder?

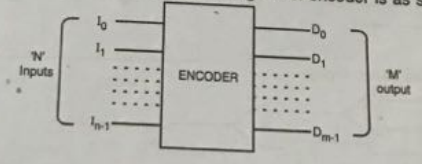
(PTU, Dec. 2009 ; May 2015, 2009)

Ans. Mechanical switches are used to drive the seven-segment display. Usually the power for LED segments is provided by an IC. The IC is called as display driver. The display driver is the same IC package as the decoder. Thus, it is commonly known as seven-segment decoder or driver.

Q 10. What is Encoder?

(PTU, Dec. 2006)

Ans. Encoder : Encoder is a combinational circuit which converts 'n' input digital word into an 'm' bit another digital word. The block diagram of encoder is as shown :



We get only one output at any time for a single unique input combination.

There are various types of encoders :

1. Decimal to BCD encoder.
2. Hexadecimal to binary encoder.
3. Octal to binary encoder.
4. Priority encoder.

Q 11. What are decoders?

(PTU, May 2006)

Ans. Decoders : Decoder is a combinational circuit which converts 'm' bits binary word

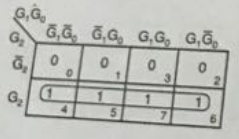
Q 7. Design 3 bit Gray Code to binary converter.

Ans. The truth table for 3 bit Gray Code to binary conversion is as shown :

Decimal Equipment	Gray Code			Binary Code		
	G_2	G_1	G_0	B_2	B_1	B_0
0	0	0	0	0	0	0
1	0	0	1	0	0	1
3	0	1	1	0	1	0
2	0	1	0	0	1	1
6	1	1	0	1	0	0
7	1	1	1	1	0	1
5	1	0	1	1	1	0
4	1	0	0	1	1	1

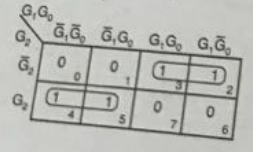
K-Maps :

For B_2 :



$\therefore B_2 = G_2$

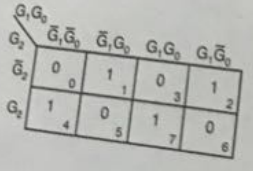
For B_1 :



$\therefore B_1 = \overline{G}_2 G_1 + G_2 \overline{G}_1$

$B_1 = G_1 \oplus G_2$

For B_0 :



$$\therefore B_0 = \overline{G}_2 \overline{G}_1 G_0 + \overline{G}_2 G_1 \overline{G}_0 + G_2 \overline{G}_1 \overline{G}_0 + G_2 G_1 G_0$$

$$= \overline{G}_2 \left(\overline{G}_1 G_0 + G_1 \overline{G}_0\right) + G_2 \left(\overline{G}_1 \overline{G}_0 + G_1 G_0\right)$$

$$= \overline{G}_2 \left(G_1 \oplus G_0\right) + G_2 \left(G_1 \odot G_0\right)$$

$$= \overline{G}_2 \left(G_1 \oplus G_0\right) + G_2 \left(\overline{G_1 \oplus G_0}\right)$$

$\therefore B_0 = G_1 \oplus G_0 \oplus G_2$

(PTU, May 2005)
) two BCD digits are
n addition of 6 (i.e.

'9' i.e. 1001. Now

8 ; Dec. 2004)
he sum of two
ith the output

— C_1

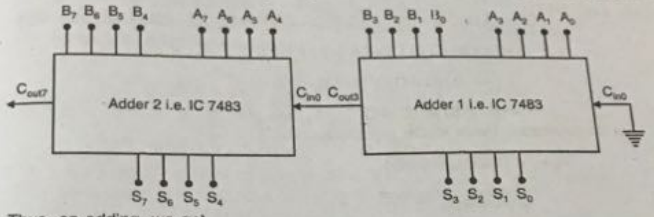
c. 2008)

4,7)

7)

Q 19. How will you form an 5 bit adder using 2 four bit adder IC's 7483. **(PTU, Dec. 2008)**

Ans. 8 bit adder can be formed by using 2 four bit adder IC's i.e. 7483. It is as shown :



Thus, on adding, we get

$$\begin{array}{r} A_7\ A_6\ A_5\ A_4\ A_3\ A_2\ A_1\ A_0 \\ B_7\ B_6\ B_5\ B_4\ B_3\ B_2\ B_1\ B_0 \\ \hline S_7\ S_6\ S_5\ S_4\ S_3\ S_2\ S_1\ S_0 \end{array}$$

Q 20. Design a circuit that will generate a odd parity bit for 4 bit input and implement it using only XNOR gates. **(PTU, May 2009)**

Ans. Following table shows the 4 bit input with odd parity output :

Inputs				Output
A	B	C	D	P_{odd}
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

Truth table shows the P_{odd} in which if number of 1's are odd the output is '0' and if number of 1's are even output is '1'. Also, when there are all zero's in the input, output is again '1'.

The K-map is as shown :

AB \ CD	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	1	0	1	0
$\bar{A}B$	0	1	0	1
AB	1	0	1	0
$A\bar{B}$	0	1	0	1

Q 16. What do you mean by BCD adder? **(PTU, May 2005)**

Ans. BCD Adder : In BCD adder (i.e. Binary Coded decimal adder) two BCD digits are added in such a way that if sum is greater than '9' (i.e. 1001 binary) then addition of 6 (i.e. 0110 binary) is done and carry is generated to next decimal position.

For example :

If the data after adding two BCD digits be : $(1010)_2$. It is greater than '9' i.e. 1001. Now add '6' i.e. 0110 in it to get the exact BCD code.

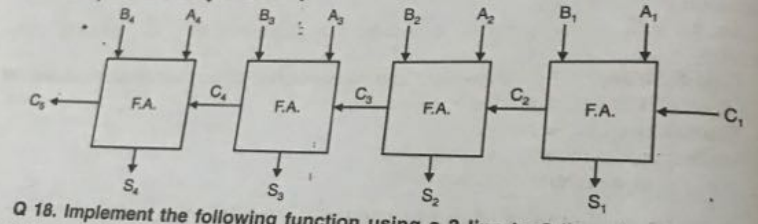
$$\begin{array}{r} 1010 \\ +\ 0110 \\ \hline 10000 \end{array}$$

Thus BCD output will be $(10000)_{BCD}$.

Q 17. What do you mean by parallel binary adder? (PTU, May 2018 ; Dec. 2004)

Ans. Parallel Binary Adder : It is a combinational circuit that gives the sum of two binary numbers in parallel. It consists of full adders connected in cascade with the output carry from one full adder connected to the input carry of the next.

4-bit parallel binary order :

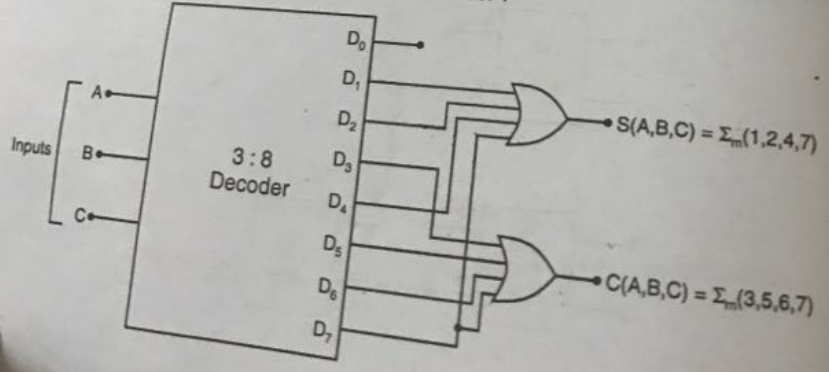


Q 18. Implement the following function using a 3 line to 8 line decoder

$S(A, B, C) = \Sigma m\ (1, 2, 4, 7)$

$C(A, B, C) = \Sigma m\ (3, 5, 6, 7)$.

Ans. Implementation using 3 line to 8 line decoder : **(PTU, Dec. 2008)**



...activated for one of the ...ers.

D_1	D_2	D_3
0	0	0
	0	0
	1	0
	0	1

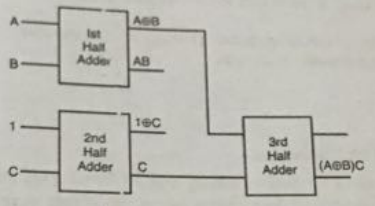
...ay 2017, 2006)

...U, May 2011)
...e (i.e. two input ...in diagram.

Carry
0
0
0
1
0
1
1
1

Q 13. Implement the Boolean function with three half adder circuit F = A'BC + AB'C. **(PTU, Dec. 2005)**

Ans. F = A'BC + AB'C = C (A⊕B)



Q 14. Define the terms decoder and demultiplexer. **(PTU, Dec. 2016, 2005)**

Ans. Decoder : Decoder is a combinational circuit which converts n-bit binary data into maximum of 2^n output lines.

So, if n = 3, we can design 3 : 8 decoder. It is also then said to be a 3 line to 8 line decoder.

Demultiplexer : It has single input and many outputs. It has only single input line, 'm' output lines and 'n' selection lines or control lines.

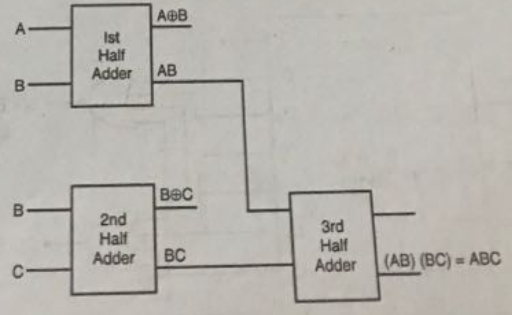
Formula used : $2^n = m$.

Where, n = number of selection lines

m = number of output lines.

Q 15. Implement the Boolean function with three half adder circuit F = ABC. **(PTU, May 2005)**

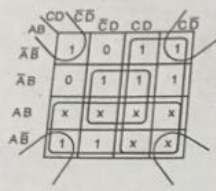
Ans. F = ABC



Put rest of the combinations as don't care i.e. 10, 11, 12,13, 14 and 15 decimal are taken as 'X'.

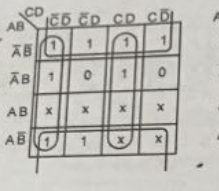
K maps are as shown for designing :

For 'a' →



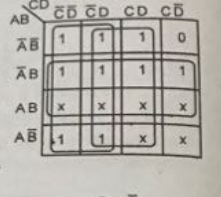
$\therefore a = A + C + BD + \bar{B}\bar{D}$

For 'b' →



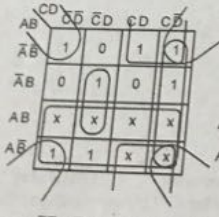
$\therefore b = \bar{B} + \bar{C}\bar{D} + CD$

For 'c' →



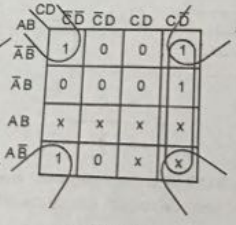
$\therefore c = B + \bar{C} + D$

For 'd' →



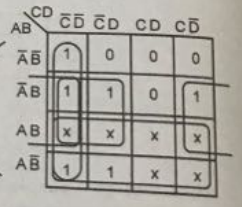
$\therefore d = \bar{B}\bar{D} + \bar{B}C + B\bar{C}D + A + C\bar{D}$

For 'e' →



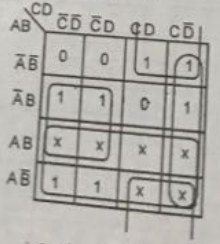
$\therefore e = \bar{B}\bar{D} + C\bar{D}$

For 'f' →



$\therefore f = A + \bar{C}\bar{D} + B\bar{C} + B\bar{D}$

For 'g' →



$\therefore g = A + B\bar{C} + \bar{B}C + C\bar{D}$

another '1'. Thus, the output

$+A\bar{B}\bar{C}D+A\bar{B}C\bar{D}$

$CD)+A\bar{B}(\bar{C}D+C\bar{D})$

xer.

PTU, Dec. 2007)

Q 22. An 8 × 1 multiplexer has inputs A, B, C connected to the selection inputs S_2, S_1, S_0 respectively. The data inputs I_0 through I_7 are as follows : $I_1 = I_2 = I_7 = 1$, $I_3 = I_5 = 0$, $I_0 = I_4 = D$ and $I_6 = \bar{D}$. (PTU, May 2007)

Ans. The select lines S_2, S_1 and S_0 are taken as A, B and C respectively.

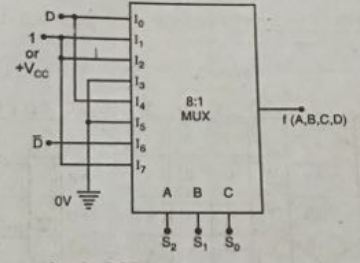
The implementation table is as shown :

	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
$\bar{D}$	0	(1)	(2)	3	4	5	(6)	(7)
D	(8)	(9)	(10)	11	(12)	13	14	(15)
Inputs for MUX ⇒	D	1	1	0	D	0	$\bar{D}$	1

($\because I_0 = I_4 = D$ and $I_6 = \bar{D}$ all others are given '0')

Thus, the function f (A, B, C, D) = Σm (1, 2, 6, 7, 8, 9, 10, 12, 15)

Implementation using 8:1 MUX is as shown



Q 23. Design a simple BCD to Seven segment decoder. (PTU, May 2005)

Ans. BCD to seven segment decoder : Let us consider it for common cathode display.

Truth table is as shown :

Decimal	Inputs				Outputs						
	A	B	C	D	a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	0	1	1

This K-map shows that none of the 1's can be shared with another '1'. Thus, the output is given by :

$$P_{odd} = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}CD + \bar{A}B\bar{C}D + \bar{A}BC\bar{D} + AB\bar{C}\bar{D} + ABCD + A\bar{B}\bar{C}D + A\bar{B}C\bar{D}$$

$$= \bar{A}\bar{B}(\bar{C}\bar{D} + CD) + \bar{A}B(\bar{C}D + C\bar{D}) + AB(\bar{C}\bar{D} + CD) + A\bar{B}(\bar{C}D + C\bar{D})$$

$$= (A \oplus B)(C \odot D) + (A \oplus B)(C \oplus D)$$

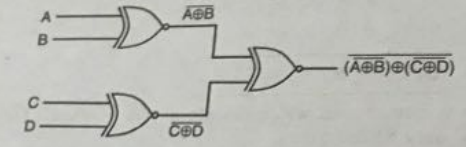
$$= (\overline{A \oplus B})(\overline{C \oplus D}) + (A \oplus B)(C \oplus D)$$

$$= (A \oplus B) \odot (C \oplus D)$$

For implementation with XNOR gates only :

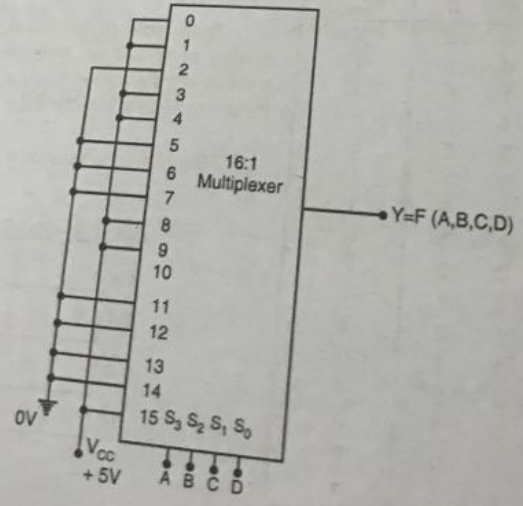
$$\bar{P}_{odd} = \overline{(A \oplus B) \odot (C \oplus D)}$$

$$= \overline{(\overline{A \oplus B}) \oplus (\overline{C \oplus D})}$$



Q 21. Implement the following Boolean function with a multiplexer.
F (A, B, C, D) = (0, 1, 3, 4, 8, 9, 15) **(PTU, Dec. 2007)**

Ans. F(A, B, C, D) = Σm (0, 1, 3, 4, 8, 9, 15)



actors and an OR gate.
TU, May 2017 ; Dec. 2004)

$B_{out} = \overline{A \oplus B} \cdot B_{in} + \overline{A}B$

Dec. 2013, 2011)
input from given
are of the many

ding. These are

U, Dec. 2008)
oes i.e. from

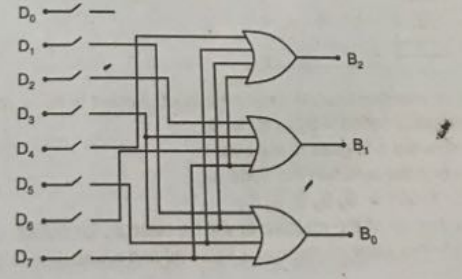
Its Truth table is given by :

Octal Inputs								Binary Outputs		
D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	B_2	B_1	B_0
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

From truth table it is clear that the logical expression will be .

$$B_0 = D_1 + D_3 + D_5 + D_7$$
$$B_1 = D_2 + D_3 + D_6 + D_7$$
$$B_2 = D_4 + D_5 + D_6 + D_7$$

Its circuit diagram is as shown :



Q 27. What is a Multiplexer Tree? Why is it needed? Draw the block diagram of a 32:1 Multiplexer Tree and explain, how is input directed to the output in this system.
(PTU, Dec. 2014 ; May 2013, 2008)

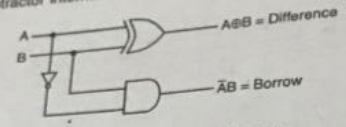
Ans. Multiplexer tree make use of multiplexer in cascading by two or more multiplexers with less number of inputs.

It is needed because more number of inputs in a multiplexer can be obtained by using cascading of multiplexers with less number of inputs.

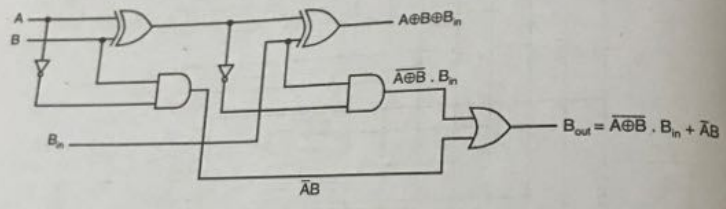
Let us take the example of 32 : 1 multiplexer tree using 16 : 1 multiplexer and 2 : 1 multiplexer.

Q 24. Implement a full subtractor with two half substractors and an OR gate. **(PTU, May 2017 ; Dec. 2004)**

Ans. *Hal subtractor internal structure is given by :*



Full subtractor using half subtractors and an OR gate.



Q 25. What is the use of multiplexer? **(PTU, Dec. 2013, 2011)**

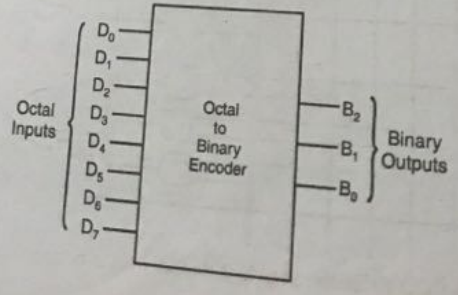
Ans. *Multiplexer is a combinational circuit which is used to give single input from given 2^n inputs, when n are the selection line or control line code, which selects are of the many inputs and produce it at the output.*

Multiplexers are used in telephone exchanges for time division multiplexing. These are also used in function generators.

Q 26. Explain the operation of octal to binary encoder. **(PTU, Dec. 2008)**

Ans. *Octal to binary encoder consists of 8 input lines and 3 output lines i.e. from formula, $2^n = M$ or $2^3 = 8$ for octal.*

Functional block diagram is as shown :



and 15 decimal are

r 'c' →

	CD	CD̄
	1	0
	1	1
	x	x
	x	x

+ D

	CD̄
	0
	1
	x
	x

D̄

Its circuit diagram is as shown :

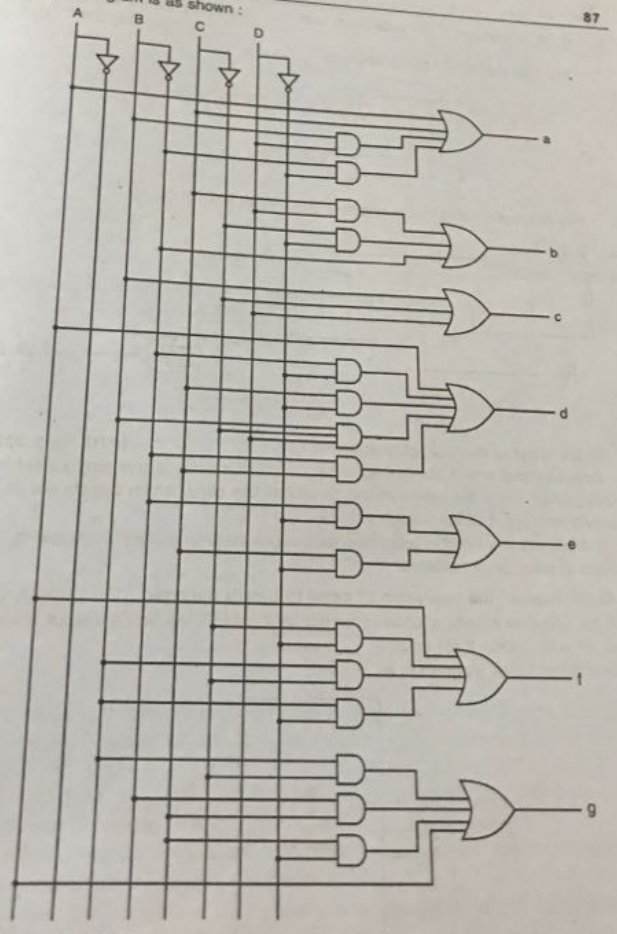
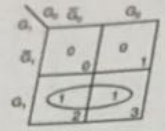
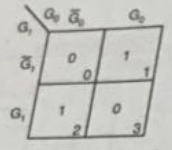


Figure shows the BCD to seven segment decoder for a common cathode type display.

Put binary outputs for B_1 and B_0 in 2-variable K-maps, we get



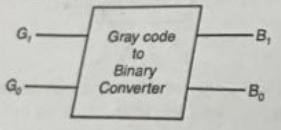
$$\therefore \quad B_1 = G_1$$

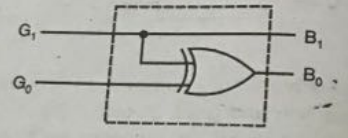


$$\therefore \quad B_0 = \overline{G}_1 G_0 + G_1 \overline{G}_0$$

$$B_0 = G_0 \oplus G_1$$

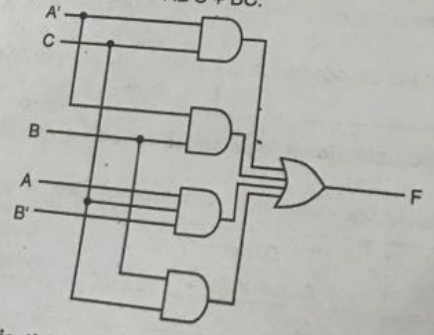
So the circuit will be :





Q 30. Draw the gate implementation of the simple fixed Boolean function : $F(A, B, C) = A'C + A'B + AB'C + BC$ using AND and OR gates. (PTU, May 2006)

Ans. $F(A, B, C, D) = A'C + A'B + AB'C + BC$.

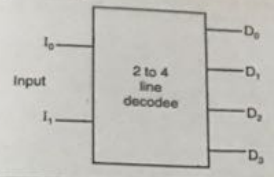


Q 31. List two applications of multiplexer. (PTU, May 2015 ; Dec. 2009)

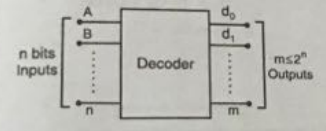
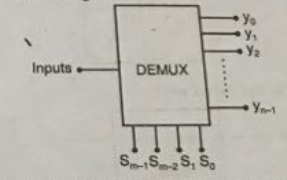
Ans. Applications of multiplexers :

1. Multiplexers are used in telephone exchanges for time division multiplexing.
2. Multiplexers are used in function generators.

Truth Table



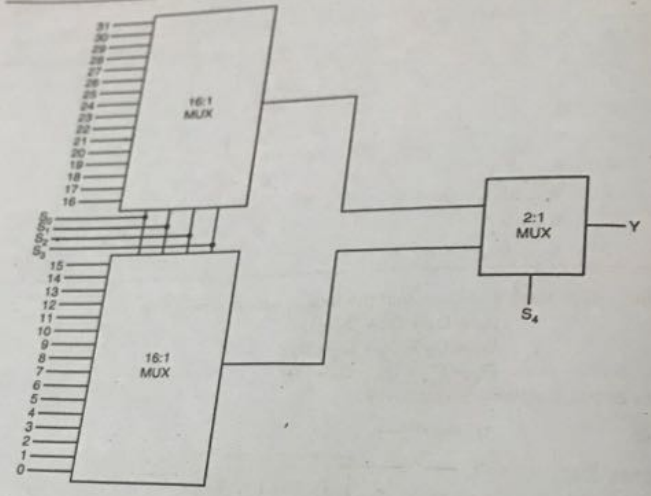
I_0	I_1	D_0	D_1	D_2	D_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Decoder	Demultiplexer
1. Block diagram : 	1. Block diagram : 
2. It receives 'n' number of coded information and gives 2^n output lines. For an 'n' to 'm' line decoder we have $m \le 2^n$ outputs.	2. It has single input line and multiple output lines. Selection lines are used to select the input at appropriate output.
3. Types of decoders are 2 to 4 line decoder, BCD to decimal decoder etc.	3. Types of demultiplexers are : 1 : 2 MUX, 1 : 4 MUX, 1 : 8 MUX and so on.
4. Number of input lines is decoder are 2 or more than 2.	4. Number of input line in demultiplexer is single.

Q 29. Design a combinational logic circuit for converting Gray code to binary. **(PTU, Dec. 2005)**

Ans. Following table shows the truth table for conversion of gray code to binary :

Equivalent Decimal	Gray Code inputs		Binary Outputs	
	G_1	G_0	B_1	B_0
0	0	0	0	0
1	0	1	0	1
3	1	1	1	0
2	1	0	1	1



The code of selection line will decide the input directed to the output Y.

When the code is 00000 = $S_4\ S_3\ S_2\ S_1\ S_0$

'O' pin is selected and goes to the output

Similarly, when the selection line code is :

$$11001 = S_4\ S_3\ S_2\ S_1\ S_0$$

The pin number 25 of the multiplexer will be selected for output.

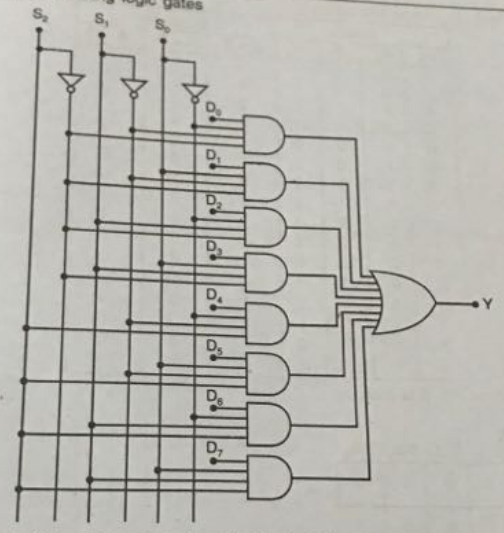
When, S_4 *is '0' the lower multiplexer is selected and when,* S_4 *is '1' the upper multiplexer is selected.*

Q 28. What is a Decoder? Compare a decoder and a demultiplexer with suitable block diagrams. **(PTU, Dec. 2014, 2013 ; May 2015, 2013, 2008)**

Ans. Decoders : Decoder is a combinational circuit which converts 'm' bits binary word into 'n' bit binary word. It is such that one of the output line will be activated for one of the possible input combinations. Demultipluters are also known as decoders.

For example : 2 to 4 line decoder is as shown ;

It has 2 inputs and 4 outputs.



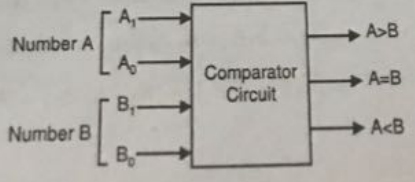
For example, if $S_2\,S_1\,S_0 = 101$, then the D_5 data input is selected and the output $Y = D_5$. The commonly used multiplexer IC's for 8:1 MUX is IC 74151 (Eight input MUX).

Q 35. How many select lines are required for a 10 to 1 MUX? (PTU, May 2011)

Ans. 4 select lines are required for 10 : 1 MUX.

Q 36. Design a comparator circuit which compares two 2 bit numbers. It has three outputs A > B, A < B and A = B. Also show that $A < B = \overline{A > B} \cdot \overline{A = B}$. (PTU, Dec. 2017 ; May 2010)

Ans. Comparation functional block diagram for two 2-bit numbers.



Q 34. Explain with block diagram what is 8 to 1 MUX. **(PTU, Dec. 2013, 2010)**

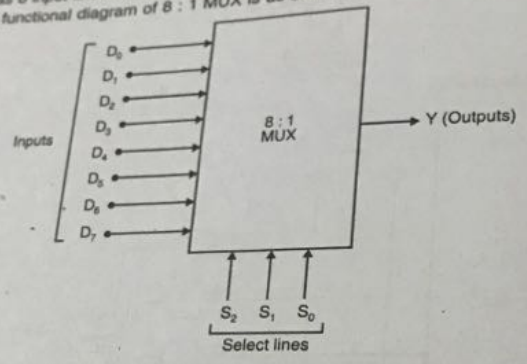
Ans. 8:1 Multiplexer (or) 8 Input MUX (or) 8:1 MUX

Formula used is $2^n = M$, where n = number of select lines and M = number of inputs, here, $M = 8$

$\therefore 2^3 = 8$ Thus, $n = 3$

It has 8 input lines and 3 select lines.

The functional diagram of 8 : 1 MUX is as shown :

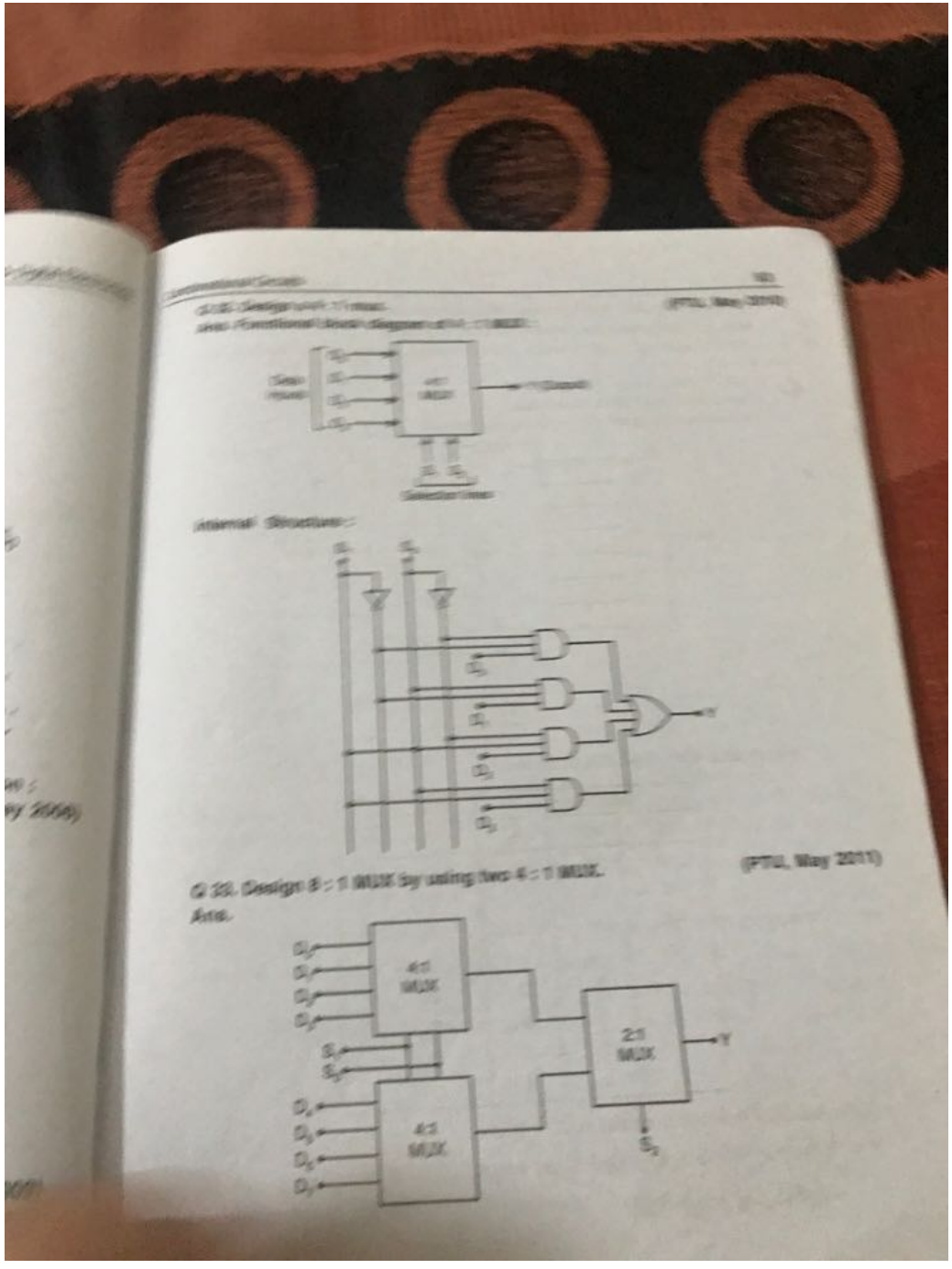


The truth table of 8 : 1 MUX is as shown

Select Input			Output
S_2	S_1	S_0	Y
0	0	0	D_0
0	0	1	D_1
0	1	0	D_2
0	1	1	D_3
1	0	0	D_4
1	0	1	D_5
1	1	0	D_6
1	1	1	D_7

Its logical SOP function is similar to 2 : 1 and 4 : 1 and is given by

$$Y = \bar{S}_2\bar{S}_1\bar{S}_0D_0 + \bar{S}_2\bar{S}_1S_0D_1 + \bar{S}_2S_1\bar{S}_0D_2 + \bar{S}_2S_1S_0D_3 + S_2\bar{S}_1\bar{S}_0D_4 + S_2\bar{S}_1S_0D_5 + S_2S_1\bar{S}_0D_6 + S_2S_1S_0D_7$$

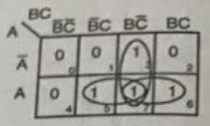


Truth table :

Inputs			Output
A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Combinational circuit can be designed if output Y is calculated using K-map, we get

For Y :



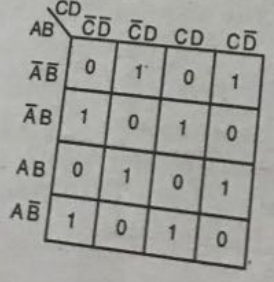
$\therefore$ $Y = AB + BC + AC$

Q 38. Design a circuit that will generate an even parity bit for 4 bit input and implement it using only NAND gates. **(PTU, Dec. 2009)**

Ans. Following table shows the 4 bit input with even parity output.

Inputs				Output
A	B	C	D	P_{even}
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

The K-map for P_{even} is as shown.

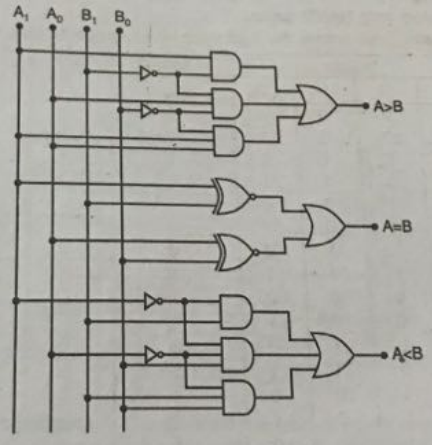


The K-map for A < B is as shown :

A_1A_0 \ B_1B_0	$\bar{B}_1\bar{B}_0$	$\bar{B}_1B_0$	B_1B_0	$B_1\bar{B}_0$
$\bar{A}_1\bar{A}_0$	0	1	1	1
$\bar{A}_1A_0$	0	0	1	1
A_1A_0	0	0	0	0
$A_1\bar{A}_0$	0	0	1	0

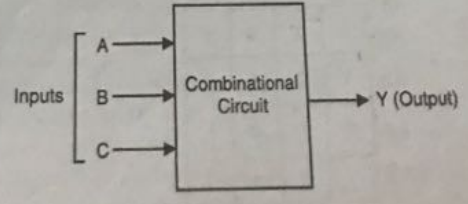
$$\therefore (A < B) = \bar{A}_1B_1 + \bar{A}_1\bar{A}_0B_0 + \bar{A}_0B_1B_0$$

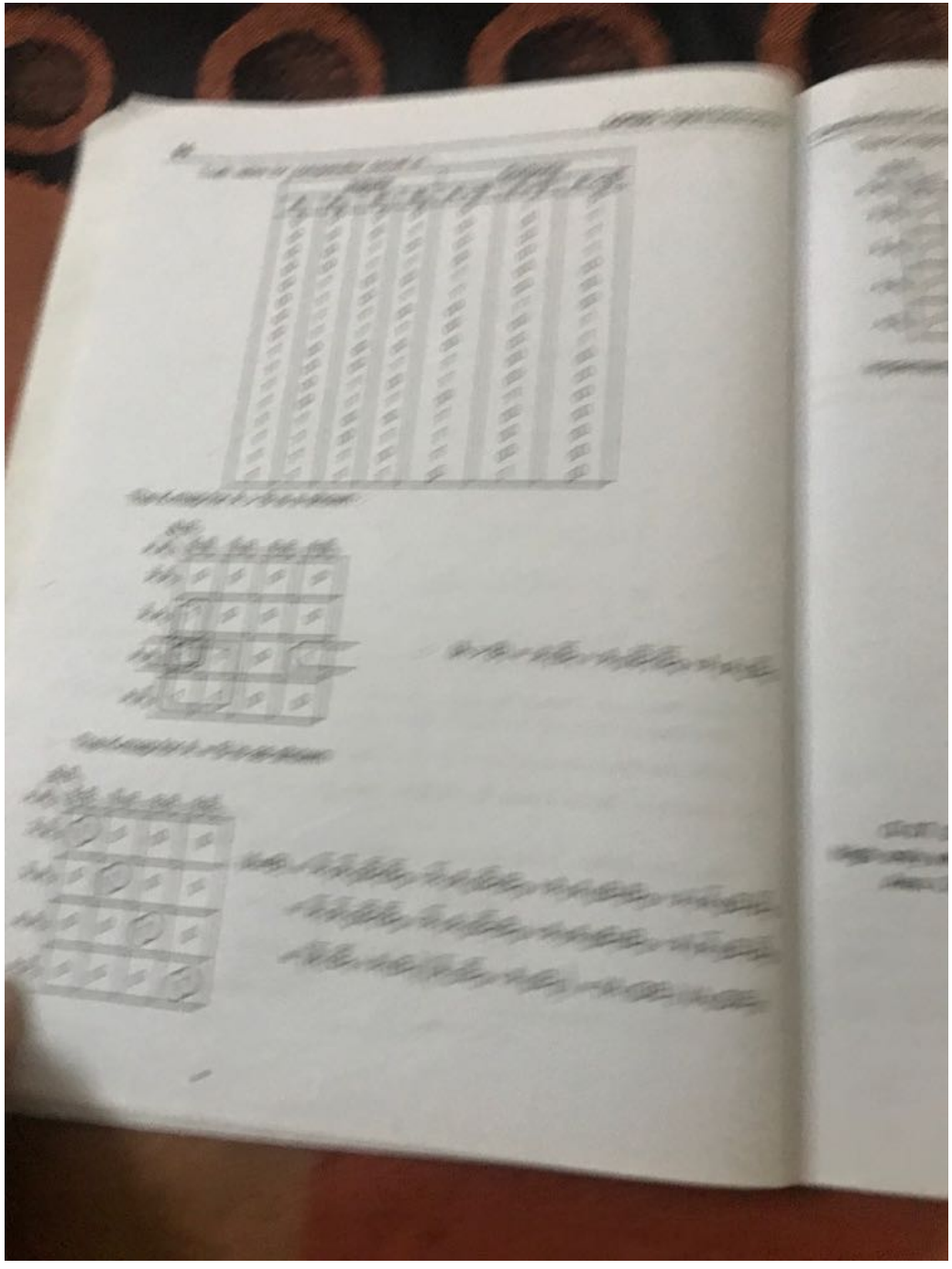
Implementation of a comparator circuit which compares two 2-bit numbers is as shown.



Q 37. Design a combinational circuit with 3 inputs and 1 output. The output is high only when more than one input is high. **(PTU, May 2010)**

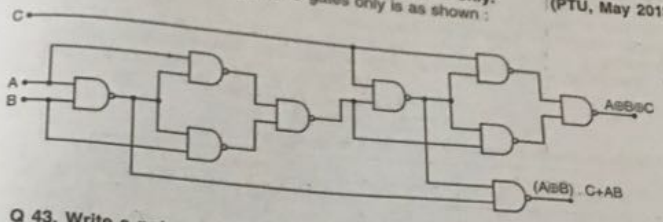
Ans. Combinational circuit functional block diagram :





Q 42. Design a full adder circuit using NAND gates only. **(PTU, May 2013)**

Ans. Full adder circuit using NAND gates only is as shown :



Q 43. Write a note on the following :
(a) Canonical POS (b) Magnitude comparator (c) Excess-3 code. **(PTU, Dec. 2014 ; May 2013)**

Ans. (a) Canonical POS :

Let $Y = AB + C$ is an expression in SOP form than,

$Y = \left(AB\overline{C} + ABC + \overline{A}\,\overline{B}C + \overline{A}BC + ABC\right)$ is a standard SOP form which is formed by taking

$Y = AB\left(\overline{C} + C\right) + \left(\overline{A} + A\right)\left(\overline{B} + B\right)$ for conversion.

Here, $AB\overline{C}$, ABC, $\overline{A}\,\overline{B}C$, $\overline{A}BC$, $A\overline{B}C$ are minterms.

So, $Y = AB\overline{C} + ABC + \overline{A}\,\overline{B}C + \overline{A}BC + A\overline{B}C$ is also called as Minterms form.

To convert in canonical form, we take standard SOP or Minterms form. In the equation $Y = AB\overline{C} + ABC + \overline{A}\,\overline{B}C + \overline{A}BC + A\overline{B}C$, there are three variables in each term. So, there are $2^3 = 8$ combinations as shown in table.

Decimal	B_2	B_1	B_0	A	B	C	Function Y	Decimal
0	0	0	0	$\overline{A}$	$\overline{B}$	$\overline{C}$	0	
1	0	0	1	$\overline{A}$	$\overline{B}$	C	1 →	→ 1
2	0	1	0	$\overline{A}$	B	$\overline{C}$	0	
3	0	1	1	$\overline{A}$	B	C	1 →	→ 3
4	1	0	0	A	$\overline{B}$	$\overline{C}$	0	
5	1	0	1	A	$\overline{B}$	C	1 →	→ 5
6	1	1	0	A	B	$\overline{C}$	1 →	→ 6
7	1	1	1	A	B	C	1 →	→ 7

Therefore, $Y = \Sigma m\,(1, 3, 5, 6, 7)$

Which is a canonical or standard form.

Q 40. Explain how division can be accomplished by repeated subtraction. **(PTU, Dec. 2011)**

Ans. For division accomplished by repeated subtraction is done by computer method of division. Suppose an 8-bit dividend is divided by a 4-bit divisior, then an MQ (multiplier/quotient) register is used in which the right-half of MQ register quotient will be formed. For remainder left-half of MQ register is used. An 8-bit dividend is first stored in MQ register and for 4-bit divisor D-flip is used. The subtraction is the started where divisor is subtracted from dividend.

The result may be negative or positive, such as :

(a) If a borrow is required, then the result is considered negative and the quotient will be of 4-bits or less which is small to be put in the right-half of MQ register.

(b) If no borrow is required, then the result is considered positive and the quotient will be greater than 4-bits. Thus, an error occurs and division using those registers cannot be completed.

Thus, the MQ register is next shifted to left by 1-bit. The bit which is shifted out is stored in a carry flag and the subtraction is done by left shift using it.

Again for negative and positive result, we have

(a) If the subtraction result is positive, then 1 is added in the LSB of MQ register and quotient is accumulated.

(b) If the subtraction result is negative, then the divisor is added to MQ register and MQ is shifted to left by 1-bit. Thus, in quotient the bit is put as 0.

This whole process continuous until the number of bits in the D register i.e. MQ register has been shifted to left by 4-bits. At last we get the quotient in right-half and remainder in left-half of MQ register.

Q 41. Design full subtractor using demultiplexer. **(PTU, May 2012)**

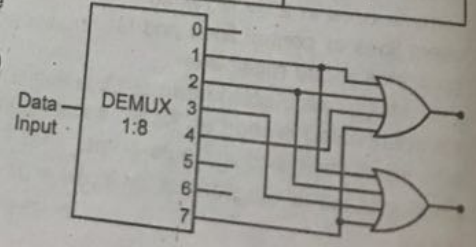
Ans. Truth table is as shown for full subtractor

Inputs			Outputs		Decimal Equivalent
A	B	C	Difference (D)	Borrow(B_0)	
0	0	0	0	0	0
0	0	1	1	1	1
0	1	0	1	1	2
0	1	1	0	1	3
1	0	0	1	0	4
1	0	1	0	0	5
1	1	0	0	0	6
1	1	1	1	1	7

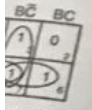
Implementation can be done by using the following, we have

f(A, B, C) for Difference, $D = \Sigma m\ (1, 2, 3, 7)$

f(A, B, C) for Borrow, $B_0 = \Sigma m\ (1, 2, 3, 7)$



ircuit can be designed
ted using K-map, we



C + AC

4 bit input and
TU, Dec. 2009)

This K-map shows that none of the 1's can be shared with another '1'. Thus, the output is given by

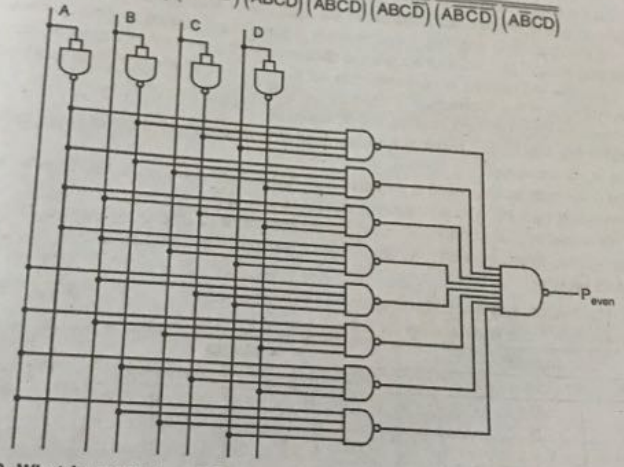
$$P_{even} = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}C\bar{D} + \bar{A}B\bar{C}\bar{D} + \bar{A}BCD + AB\bar{C}\bar{D} + ABC\bar{D} + A\bar{B}\bar{C}\bar{D} + A\bar{B}CD.$$

For implementation using only NAND gates, we have

$$P_{even} = \overline{P_{even}}$$

$$= \overline{\bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}C\bar{D} + \bar{A}B\bar{C}\bar{D} + \bar{A}BCD + AB\bar{C}\bar{D} + ABC\bar{D} + A\bar{B}\bar{C}\bar{D} + A\bar{B}CD} \quad \left(\because \bar{\bar{A}} = A\right)$$

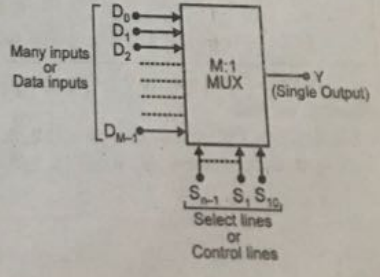
$$= \overline{(\bar{A}\bar{B}\bar{C}\bar{D})}\,\overline{(\bar{A}\bar{B}C\bar{D})}\,\overline{(\bar{A}B\bar{C}\bar{D})}\,\overline{(\bar{A}BCD)}\,\overline{(AB\bar{C}\bar{D})}\,\overline{(ABC\bar{D})}\,\overline{(A\bar{B}\bar{C}\bar{D})}\,\overline{(A\bar{B}CD)}$$



Q 39. What is multiplexer? Explain with the help of an example. **(PTU, May 2012)**

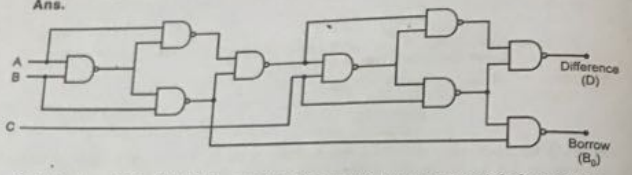
Ans. Multiplexer are the universal circuits like NAND and NOR gates. Multiplexer means 'many into one'. It selects one input out of multiple inputs and produce it at the output. The selection of the input is done by selection lines. Formula used in $2^n = M$, where n = number of select lines or control lines and M = number of input lines to the multiplexer.

Multiplexer is also known as 'Data Selector'. It is abbreviated in short as 'MUX'. It has several data input lines and a single output line. The functional block diagram of multiplexer is as shown



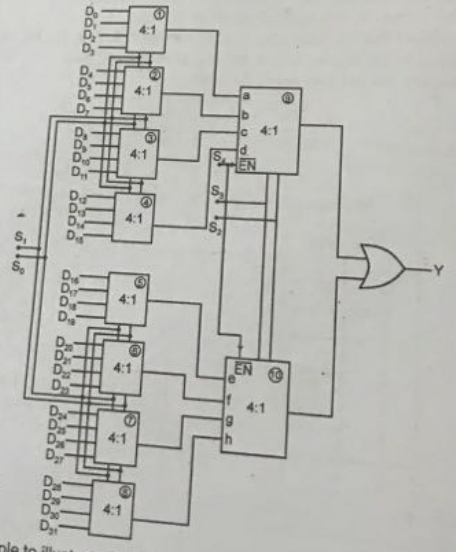
Q 46. Design a full Subtractor circuit using NAND gates only. (PTU, Dec. 2014)

Ans.



Q 47. Design a 32 to 1 Multiplexer using 4 to 1 Multiplexer and explain its working. (PTU, May 2016)

Ans. 32 : 1 MUC using 4 : 1MUX is as shown



Lets take an example to illustrate the above implementation

$S_4S_3S_2S_1S_0$ Output Y

ABCDE

00101 D_5

When $S_Y = 0$, 9th multiplexer will enabled and 10th MUX will be disabled. $S_3\ S_2 = 01$, Which

Addition of $(0110)_{BCD}$ and $(0011)_2$ is given as :

$$\begin{array}{r} 0\,1\,1\,0 \\ +\,0\,0\,1\,1 \\ \hline 1\,0\,0\,1 \text{ excess-3} \end{array}$$

Example : Obtain Excess-3 code of $(48)_{10}$.

Solution. $(48)_{10} \rightarrow \underbrace{(0100}_{}\ \underbrace{1000)_{BCD}}_{}$

$$\begin{array}{r} 0011\ 0011 \\ \hline (0011\ 0011)_{excess\text{-}3} \end{array}$$

Note : Excess-3 code is self complementing code as 1's complement of an excess-3 code is an excess-3 for 9's complement of the decimal.

Example : Show the self complement nature of excess-3 code.

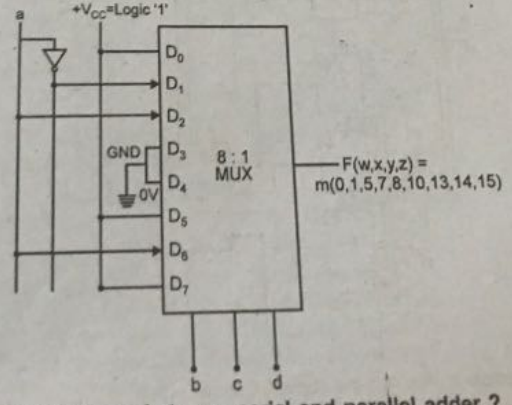
Solution. Lets take the decimal $(6)_{10}$. 1's complement of $(6)_{10} \Rightarrow (0110)_2 = (1001)_2$. It's excess-3 code is 1001 and the 1's complement of $(1001)_2$ is $(0110)_2$.

Which is the excess-3 of 9's complement of (0110).

Q 44. Implement the function f (w, x, y, z) = m (0, 1, 5, 7, 8, 10, 13, 14, 15) using two 8-way multiplexers with an active low enable, plus an OR gate. (PTU, May 2014)

Ans. Implement the function using 8:1 MUX

	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
$\bar{a}$	⓪	①	2	3	4	⑤	6	⑦
a	⑧	9	⑩	11	12	⑬	⑭	⑮
MUX input	1	$\bar{a}$	a	0	0	1	a	1

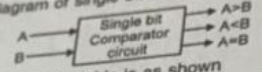


Q 45. What is difference between serial and parallel adder ? (PTU, Dec. 2015)

Ans. Serial adder require are full adder for one additional bit while parallel adders requires n-full adder for n-bit addition.

(b) Magnitude comparator : Comparator compares two binary numbers. Lets take an example of magnitude comparator for comparison of single bit binary numbers. Suppose, the input variables be A and B, thus the outputs are A > B, A = B and A < B for comparison respectively.

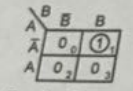
The functional block diagram of single bit magnitude comparator is as shown



Single or one bit comparator truth table is as shown

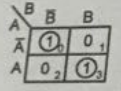
Inputs		Outputs		
A	B	A < B	A = B	A > B
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

K-map for A < B ⇒



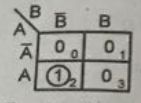
∴ For A < B output is $\bar{A}B$

K-map for A = B ⇒



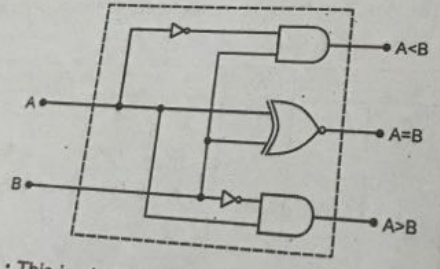
∴ A = B output is $\bar{A}\bar{B} + AB = A \otimes B$

K-map for A > B ⇒



∴ For A > B output is $A\bar{B}$

The circuit diagram for single bit or one bit comparator is as shown



(c) Excess-3 code : This is obtain by addition of three i.e., $(0011)_2$ to the BCD. Excess-3 code is related to BCD 8421 code because of its binary coded decimal nature i.e., the group of four bits in an excess-3 code is equal to a specific decimal digit.

Example : Obtain Excess-3 code of $(6)_{10}$

Solution. Convert

$(6)_{10}$ to BCD

$(6)_{10} \rightarrow (0110)_{BCD}$

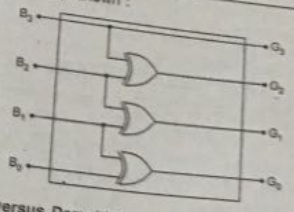
gray convertor. (PTU, May 2018)

	Gray Code		
	G_2	G_1	G_0
	0	0	0
	0	0	1
	0	1	1
	0	1	0
	1	1	0
	1	1	1
	1	0	1
	1	0	0
	1	0	0
	1	0	1
	1	1	1
	1	1	0
	0	1	0
	0	1	1
	0	0	1
	0	0	0

$B_3 \oplus B_2$

$\oplus B_0$

implementation of circuit is as shown :



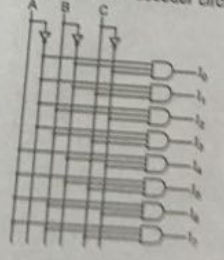
Q 52. Multiplexer versus Demultiplexer. (PTU, May 2018)

Ans.

DMUX	MUX
1. It has an input and many outputs.	1. It has many inputs and one output.
2. It is also known as data distributor.	2. It is also known as data selector.
3. OR gate is not required.	3. OR gate is required at the output stage.
4. IC no. of 1 : 16 DEMUX is 74154.	4. IC no. of 16 : 1 MUX is 74150.

Q 53. Draw logic diagram of 3-line to 8-line decoder. (PTU, May 2019)

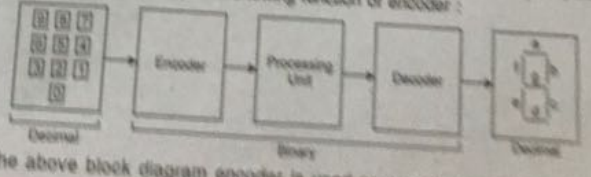
Ans. 3 line to 8 line decoder circuit :



A	B	C	Output
0	0	0	I_0
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	0	1	I_5
1	1	0	I_6
1	1	1	I_7

Q 54. With a neat block diagram explain the function of encoder. Explain parity checker. (PTU, May 2019)

Ans. Block diagram of system showing function of encoder :



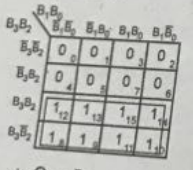
In the above block diagram encoder is used as a pocket calculator. It translates

Q 51. Design and implement a 4 bit binary to gray convertor. (PTU, May 2018)

Ans. Truth table is as shown :

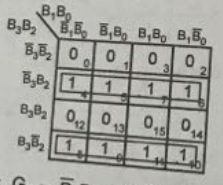
Decimal Equivalent	Binary Code				Gray Code			
	B_3	B_2	B_1	B_0	G_3	G_2	G_1	G_0
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1
2	0	0	1	0	0	0	1	1
3	0	0	1	1	0	0	1	0
4	0	1	0	0	0	1	1	0
5	0	1	0	1	0	1	1	1
6	0	1	1	0	0	1	0	1
7	0	1	1	1	0	1	0	0
8	1	0	0	0	1	1	0	0
9	1	0	0	1	1	1	0	1
10	1	0	1	0	1	1	1	1
11	1	0	1	1	1	1	1	0
12	1	1	0	0	1	0	1	0
13	1	1	0	1	1	0	1	1
14	1	1	1	0	1	0	0	1
15	1	1	1	1	1	0	0	0

K-maps for G_3



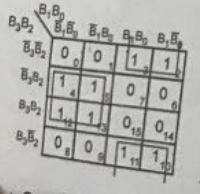
$\therefore G_3 = B_3$

K-maps for G_2



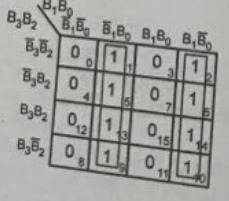
$\therefore G_2 = \bar{B}_3B_2 + B_3\bar{B}_2 = B_3 \oplus B_2$

K-maps for G_1



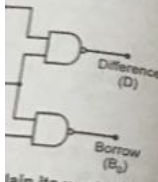
$\therefore G_1 = \bar{B}_1B_2 + B_1\bar{B}_2 = B_1 \oplus B_2$

K-maps for G_0



$\therefore B_0 = \bar{B}_1B_0 + B_1\bar{B}_0 = B_1 \oplus B_0$

only. (PTU, Dec. 2014)



lain its working.
(PTU, May 2016)

means 2nd line of each multiplexer i.e., 9th and 10th will be at the output. But 9th MUX is enabled and 10th is disabled. Also $S_1S_0 = 01$, which means 2nd line of each MUX i.e., MUX 1to MUX 8 will be enabled. Thus, D_1, D_5, D_9 and D_{13} will be at the input of MUX 9. Also, 2nd line of MUX 9 i.e. 'b' will be at the output of MUX 9. 2nd line is from MUX 2 i.e. D_5. Thus, D_5 will be the output of MUX 9, further MUX 10 is disabled due to enable signal and we get D_5 at the output Y

$\therefore \quad Y = D_5 + 0 = D_5$

Q 48. How many select lines are required for 10 to 1 MUX ? (PTU, Dec. 2016)

Ans. For 10 to 1 MUX the select lines required can be calculated by using. $2^n = M$ formula. Where 'n' are the number of select lines used and 'M' are the data input lines.

$\therefore \quad 2^n = 10$

Put n = 4, we get

$2^4 > 10$ and for n = 3, we have $2^3 < 10$

Thus, 4 select lines are required.

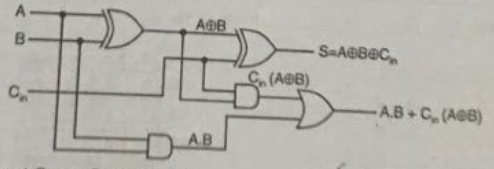
Q 49. Explain the working of carry look ahead adder. (PTU, Dec. 2016)

Ans. 3-bit look ahead adder : The 3 bit look ahead carry adder speeds up the process by eliminating ripple carry delay. It examines all the input bits simultaneously and generates carry-in-bits for all stages simultaneously. It is done with two additional functions carry generate and carry propagate function.

The carry generate function indicates as to when a carry-out would be generated by full-adder. A carry-out is generated only when both the inputs bits are 1. This condition is expressed as the AND function of the two bits A and B.

Carry generate (CG) = A . B

Carry propagate (GP) = A ⊕ B



and carry out $C_{out} = C_G + C_P - C_{in}$

The other expressions are :

$$C_{out1} = CG_0 + CP_0 . C_{in}\,0$$
$$C_{out1} = CG_1 + CP_1 . C_{in}\,1$$
$$= CG_1 + CP_1 . C_{out}\,0$$
$$= CG_1 + CP_1\,(CP_0 . C_{in0} + CG_0)$$
$$= CG_1 + CP_1 . CG_0 + CP_1 . CP_0 . C_{in}\,0$$

Similarly, $C_{out2} = CG_2 + CP_2 . CG_1 + CP_2 . CP_1\,CG_0 + CP_2 . CP_1 . CP_0 . C_{in}\,0$

Q 50. Calculate the number of select lines in 16 to 1 multiplexer ? (PTU, May 2017)

...elect lines in 16 to 1 multiplexer is given by $2^n = M$, where n = no. of ...input lines.

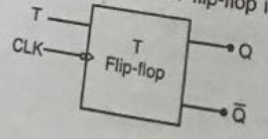
...input lines will be used for the multiplexer having '4' select lines.

- Toggle state is that in which the output changes from its previous state with every clock pulse, when the inputs are $J = K = 1$.
- Master slave flip-flop overcomes the problem of race around condition, which is common in J-K flip-flops using level clocks.
- Register is a set of flip-flops used to store binary data or information.
- The registers in which shifting of data takes place are called as shift registers.
- Types of shift registers are :
  SISO i.e. Serial in Serial Out.
  SIPO i.e. Serial in Parallel Out.
  PISO i.e. Parallel in Serial Out.
  PIPO i.e Parallel in Parallel Out.
- Bidirectional shift register is used to shift data from left to right or right to left.
- Universal shift register performs similar function as that of bidirection shift register in addition to it data can be shifted in and out in serial form or in parallel form.
- Counter is a device used to count clock pulses or number of events.
- Counter types are :
  Asynchronous Counters
  Synchronous Counters.
- Asynchronous counters are those in which clock is not simultaneous i.e. output of Ist flip flop acts as clock to the next and so on.
- Synchronous counters are those in which clock is simultaneous i.e. common to all the flip flops.
- Modulus counters are those which passes through number of states before returning to the starting state.
- A twisted ring counter is known as Johnson counter.
- Monostable multivibrator has only one stable state. It is also called as one-shot multivibrator.
- Astable multivibrator has no stable states. It is called as free-running multivibrator.
- Moore circuit is that in which output depends only on the present state of flip-flops.
- Mealy circuit is that in which output depends on both the present state of the flip-flops and the external inputs.

QUESTION-ANSWERS

Q 1. Explain T-flip-flop with suitable internal structure. **(PTU, May 2016)**

Ans. The functional block diagram of T flip-flop is as shown in fig.



rough encoder. Thus, encoder
cessing takes places in the
decoder. The decoder convert
man reference.
ransmission of binary data or
the transmitter is known as
receiver is known as parity
r is for odd parity we have
hown :

	P_{odd}
	1
	0
	0
	1

Chapter 5

Sequential Circuits

Contents

Flip flops SR, JK, T, D and Master slave, Excitation table, Edge triggering, Level Triggering, Realization of one flip flop using other flip flops. Asynchronous/Ripple counters, Synchronous counters, Modulo-n counter, Ring Counters. Design of Synchronous counters: state diagram, Circuit implementation. Shift registers.

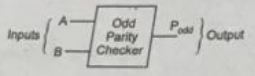
POINTS TO REMEMBER

- Flip-flop is a sequential circuit or device which is used to store single bit of information or data i.e. either '0' or '1'. Single flip-flop stores single bit at a time.
- Flip-flop is a bistable multivibrator as it has two stable states.
- An unclocked flip-flop is called a latch. A latch is that circuit which is constructed using two cross-coupled NAND gates or NOR gates.
- NOR gate S-R latch is called an active High SR latch.
- NAND gate S-R latch is called an active Low SR latch.
- Flip-flops may be level-triggered or edge-triggered level-triggered are :
  High level triggered
  Low level triggered
  Edge-triggered are : Positive edge triggered
  Negative edge triggered
- Types of flip-flops are :
  RS, JK, D and T type.
- D flip flop is also called as transparent latch as its output follows the input when the clock is high.
- J-K flip-flop is the most widely used of all flip-flops.
- For SR flip-flop :
  When, S = R = 0, there is NO change condition.
  When, S = 1, R = 0, there is SET state.
  When, S = 0, R = 1, there is RESET state.
  When, S = R = 1, there is invalid state.
- For J-K flip-flop :
  When, J = K = 0, there is NO change condition.
  When, J = 1, K = 0, there is SET state.
  When, J = 0, K = 1, there is RESET state.
  When, J = K = 1, there is Toggle state.

electronically from decimal device such as keypad to binary through encoder. Thus, encoder converts human language to machine language. Then processing takes places in the processing unit which provides the output for decoding to the decoder. The decoder convert back binary to decimal and the 7-segment will display it for human reference.

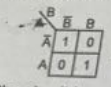
Parity Checker : A parity bit used to detect errors during transmission of binary data or information. The digital circuit that generates the parity bit in the transmitter is known as parity generator and the digital circuit that checks the parity in the receiver is known as parity checker. Let us design 2-bit parity checker. Let the parity checker is for odd parity we have

Truth table is as shown :



A	B	P_{odd}
0	0	1
0	1	0
1	0	0
1	1	1

K-map for P_{odd} is as shown :



$\Rightarrow P_{odd} = \bar{A}\,\bar{B} + AB = A \odot B$

Thus, the circuit is as shown :

□□□

A+B=

Chapt

5

Contents

Flip flops SR,
Realization of
counters, Mod
Circuit implem

- Flip-flop is
  data i.e. e
- Flip-flop is
- An uncloc
  two cross-
- NOR gate
- NAND ga
- Flip-flops
  High level
  Low level
  Edge-trigg
  Negative
- Types of
  RS, JK, D
- D flip flop
  is high.
- J-K flip-flo
- For SR fli
  When, S
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  When, S
  When, S
- For J-K fl
  When, J
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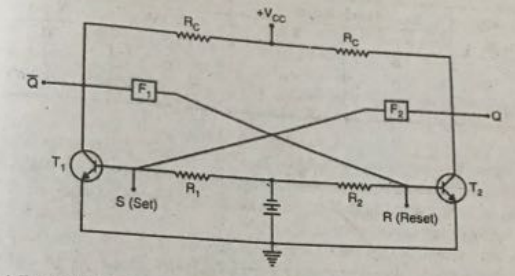
Q 9. Draw the general block diagram of multivibrator.

Ans. It is as shown :



F_1 and F_2 are the options for the connections of passive components according to the type of multivibrator to design.

For example :

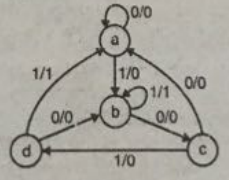
(a) Astable Multivibrator : $F_1 = C_1$ and $F_2 = C_2$.

(b) Monostable Multivibrator : $F_1 = C$ and $F_2 = R$.

(c) Bistable Multivibrator : $F_1 = F_2$ = Paraliel combination of R and C of different values.

Q 10. For the given state diagram, draw the state reduction diagram.

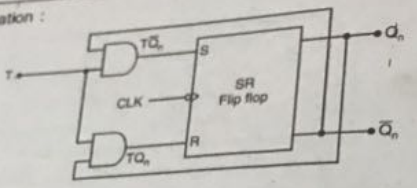
State Diagram :



Ans. State table is as shown :

Present State	Next States		Output	
	X = 0	X = 1	X = 0	X = 1
a	a	b	0	0
b	c	b	0	1
c	a	d	0	0
d	b	a	0	1

Implementation :



Q 3. Give applications of JK flip-flops.

Ans. 1. J-K flip-flops are used in shift registers.
2. J-K flip-flops are used in counters.

Q 4. Give difference between latch and flip-flop.

Ans.

Latch	Flip-flops
1. Latch has an enable input.	1. Flip-flops has a clock signal.
2. As long as enable input is active, the latch output will keep changing according to input.	2. Flip-flop samples its inputs and changes its outputs only at a particular instant of time i.e. when clock is provided.

Q 5. How race around condition can be eliminated? **(PTU, May 2016)**

Ans. Race around condition can be eliminated in JK latch by two ways :
1. Using the edge triggered J-K flip-flop.
2. Using the master slave J-K flip-flop.

Q 6. What is a Glitch?

Ans. Glitch is a short duration pulse or spike that appears in the outputs of a counter with MOD number $<2^n$.

Q 7. How many flip-flops are required to count 16 clock pulses? Why?

Ans. To count 'n' clock pulses 'm' flip-flops are required, where,

$$n \leq 2^m$$

Thus, for 16 clock pulses to count, 4 flip-flops are required as $2^4 = 16$.

Q 8. Write applications of shift registers. **(PTU, May 2018)**

Ans. 1. It is used for temporary storage of data.
2. It is used as parallel to serial converter.
3. It can be used as a ring counter.
4. It can be used for the multiplication and division arithmetics.
5. It is used as a serial to parallel converter.
6. It can be used as a delay line.
7. It can be used as a Johnson counter or twisted ring counter.

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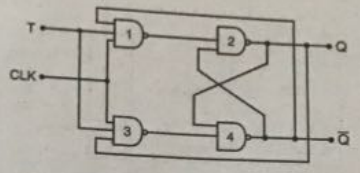
TU, May 2016)

T flip-flop is known as Toggle flip-flop



T	CLK	Q_{n+1}
0	↓	No change
1	↓	Toggle

When, T = 1 both NAND Gates 1 and 2 gets high

A T flip-flop is designed by combining both the inputs of Gate 1 and 2 together. Thus, when J = K = 0, Q have same previous state i.e. hold state or no change state. When J = K = 1, Q have toggle state i.e. invert the previous state.

Q 2. Convert SR flip-flop to T flip-flop.

Ans. Firstly write the truth table for SR to T flip-flop as shown :

T	Inputs		Outputs	
	Present State Q_n	Next State Q_{n+1}	S	R
0	0	0	0	X
0	1	1	X	0
1	0	1	1	0
1	1	0	0	1

K maps for S & R are :

For S :

T \ $Q_n\ \overline{Q}_n$	Q_n	$\overline{Q}_n$
$\overline{T}$	0	X
T	1	0

$\therefore S = T\overline{Q}_n$

For R :

T \ $Q_n\ \overline{Q}_n$	Q_n	$\overline{Q}_n$
$\overline{T}$	X	0
T	0	1

$\therefore R = TQ_n$

∴ Time taken to load serially the eight bit will be given by

$$= n \times \frac{1}{f_{CLK}}$$

$$= 8 \times \frac{1}{2 \times 10^6} = 4 \times 10^{-6} = 4\ \mu sec.$$

(PTU, Dec. 2006)

Q 17. What is flip-flop?

Ans. Flip-flop : Flip-flop is a sequential circuit which is used to store single bit of informaton at a time i.e. either '1' or '0' at a time. It has two stable output states. It can stay in any one of the two stable states unless state is changed by applying external inputs. Thus, it acts as a basic memory element for storage of data in binary form.

There are various types of flip-flops :

1. S-R flip flop
2. J-K flip-flop
3. D-type flip flop
4. T-type flip-flop

Q 18. Explain about multivibrator. **(PTU, Dec. 2006 ; May 2006)**

Ans. Multivibrators : Most of the digital circuits or systems need some kind of a timing waveform for example, all clocked sequential system required a source of trigger pulses. A timing circuit which produces a rectangular waveforms are referred to as multivibrators. There are different types of multivibrators such as :

1. Astable Multivibrator
2. Monostable Multivibrator
3. Bistable Multivibrator.

Q 19. What is shift register? **(PTU, Dec. 2017, 2012 ; May 2012, 2006)**

Ans. Shift register : A register is capable of shifting its binary information either from right to left or left to right is known as shift register. It consists of flip-flops connected in cascade. All flip-flops receive a common clock pulse which causes the shift from one stage to the next stage.

It is of four basis types :

1. Serial in serial out register
2. Serial in parallel out register
3. Parallel in serial out register
4. Parallel in parallel out register.

Bi-directional shift register and Universal shift registers are also used for different applications.

Q 20. Give the logic diagram and characteristic table of clocked D flip-flop. **(PTU, Dec. 2016, 2005)**

Ans. Clocked D Flip-flop :

Output (Y)	
	X = 1
	0
	1
	1

(PTU, May 2009)

s self-starting type. So,
into a valid state after

(PTU, May 2009)

so that the output will
It is as shown in fig.

t or clear inputs
output Q will look

Q 13. A presettable counter has eight flip-flops. If the preset number is 125, what is the modulus? (PTU, Dec. 2007)

Ans. $2^8 = 256$

$\therefore \quad 256 - 125 = 131$

Thus, MOD – 131.

Q 14. Differentiate between synchronous and asynchronous counters. (PTU, May 2015, 2014, 2011, 2010 ; Dec. 2017, 2013, 2007)

Ans.

Synchronous Counters	Asynchronous Counters
1. Simultaneous clock signal is given to all the flip-flops connected in synchronous counters.	1. Clock is provided to first flip-flop and the output of first flip-flop acts as clock to the second flip-flop and so on.
2. Speed is fast as no clock delay is provided to flip-flops.	2. Speed is slow as compared to synchronous counters as clock signal is delayed for other flip-flops except the first one.
3. Circuit is complex.	3. Circuit is simple.
4. Cost is more as additional circuitry is required.	4. Cost is less as compared to synchronous counters.

Q 15. Differentiate between sequential and combination circuits. (PTU, May 2018, 2013, 2012, 2011, 2007 ; Dec. 2017, 2014, 2010)

Ans.

Combinational Circuits	Sequential Circuits
1. Output depends only on the past values of input.	1. Output depends on the present and past values of input.
2. Feedback path is not used in combinational circuits.	2. Feedback path is used for sequential circuits.
3. Memory element is not present.	3. Memory element is present.
4. Clock is not used in combinational circuits.	4. Clock is used in sequential circuits.
5. Circuit is simple.	5. Circuit is complex.
6. Examples of combinational circuits are : Adders, subtractors, code converters, comparators, multiplexer, de-multiplexer, decoder, encoder, etc.	6. Examples of sequential circuits are : Flip-flops, counters, registers etc.

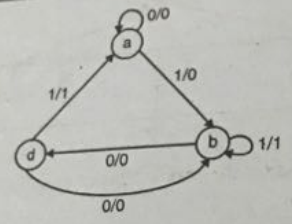
Q 16. The clock frequency is 2MHz. How long will it take to serial load the eight bit shift register? (PTU, May 2007)

Ans. $f_{CLK} = 2MHz$

$n = 8$

For modified reduced state diagram :

Present State	Next States		Output (Y)	
	X = 0	X = 1	X = 0	X = 1
a	a	b	0	0
b	d	b	0	1
d	b	a	0	1

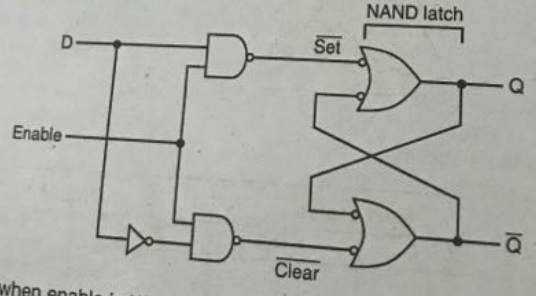


Q 11. What do you mean by self starting type counter? **(PTU, May 2009)**

Ans. Whenever there is no problem of lock out then the counter is self-starting type. So, if any time the counter goes into an invalid state, it comes out and goes into a valid state after application of one clock pulse.

Q 12. Why is gated D latch called transparent latch? **(PTU, May 2009)**

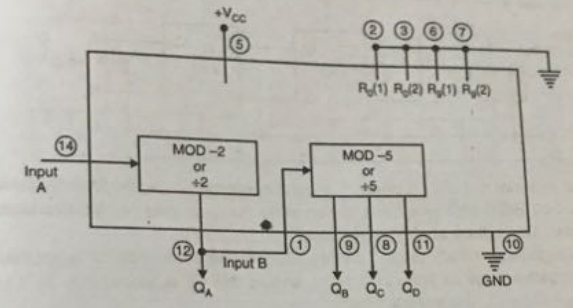
Ans. The edge triggered D flip-flop uses an edge-detector circuits so that the output will respond to D input only when the active transition of clock takes place. It is as shown in fig.



From fig. when enable is '1', the D input will given a '0' at either the $\overline{set}$ or $\overline{clear}$ inputs of NAND latch. Thus, Q becomes same as D. Thus, when enable is '1' the output Q will look exactly like D. Hence, the D latch is said to be transparent latch.

Q 26. Draw the circuit diagram of a mod-5 counter and convert it into decade counter. **(PTU, May 2015 ; Dec. 2013, 2007)**

Ans. IC 7490 as decade counter is used. It is as shown :



The Q_A output is externally connected to input B. It acts as clock input to mod-5 ripple counter. Following table shows the MOD-10 configuration using MOD-2 and MOD-5 counters :

MOD-5 counter outputs			Output	Clock	Count
Q_D	Q_C	Q_B	Q_A		Q_D Q_C Q_B Q_A
0	0	0	0	0	0
0	0	0	1	1↓	1
0	0	1	0	2↓	2
0	0	1	1	3↓	3
0	1	0	0	4↓	4
0	1	0	1	5↓	5
0	1	1	0	6↓	6
0	1	1	1	7↓	7
1	0	0	0	8↓	8
1	0	0	1	9↓	6

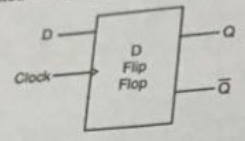
MOD-5 counter outputs

FFA toggles with clock edge

After 1001 if reset to 0000.

Q 22. Describe the advantages of using PLA over ROM for realizing some Boolean functions. **(PTU, May 2005)**

Ans. Clocked D-flip-flop :



Characteristic Table :

CLK	D	Q_n
↑	0	0
↑	1	1

Q 23. What is the role of Binary Counter? **(PTU, May 2005)**

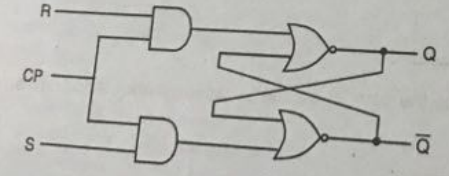
Ans. *Binary counter counts the clock pulses or number of events. The number of states in a binary counter are given by 2^n. Thus, for 3 bits $2^3 = 8$, eight states are counted by the counter.*

Ripple counters are examples of binary counter i.e. up-down ripple counter.

Q 24. Give the logic diagram and characteristic table of a clocked RS flip-flop. **(PTU, Dec. 2004)**

Ans.

Clocked RS Flip Flop :



Characteristic Table

R	S	Q_{n+1}
0	0	No change
0	1	1 i.e. Set
1	0	0 i.e. Reset
1	1	Indeterminate

Q 25. What is the role of BCD counter? **(PTU, Dec. 2004)**

Ans. A BCD counter is a binary coded decimal counter. It counts in binary coded decimal i.e. from 0000 to 1001 and then back to 0000. It is similar to decade counter.

BCD counter can be cascaded to form a counter for decimal numbers of any length.

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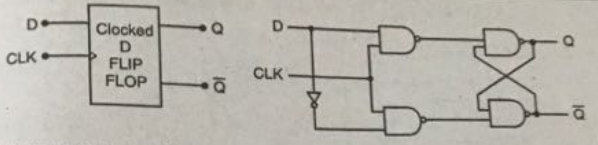


Differentiator is used in clock circuit.
For positive edge triggered clock

Clock Input	D Input	Q_{n+1} Output
↑	0	0
↑	1	1

Thus, Q_{n+1} follows the input D.

Q 21. What is the role of Binary ripple counter? **(PTU, Dec. 2005)**

Ans. Ripple counter is also known as asynchronous counter. It is used to count clock pulses. Ripple counter may be up and down. The role of up ripple counter is to count from 0 to n. Where, 'n' is a binary number of m bits (m = 0, 1, 2, ... n).

For example for 2 bit binary ripple up counter the table is as shown :

UP

Binary	Counting
0 0	0
0 1	1
1 0	2
1 1	3

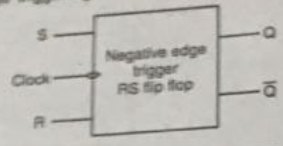
With each passage of clock pulse the counter counts up as clear from table. Similarly, for down counter 2 bit we get :

Down

Binary	Counting
1 1	3
1 0	2
0 1	1
0 0	0

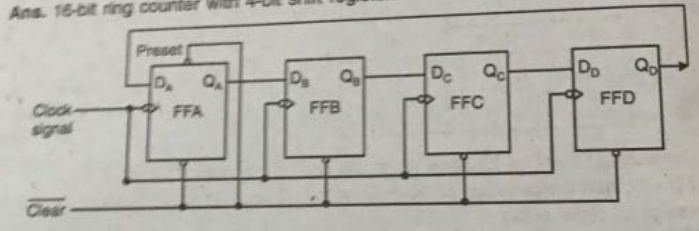
2. Negative Edge-Triggered flip-flops : In negative edge triggered flip-flops the clock samples the input lines at the negative edge or falling edge of the clock-pulse.

A negative edge-triggered flip-flop is as shown in fig. in which a small circle in the clock indicates negative edge triggering.



Q 30. Design a 4 bit ring counter with 4 bit shift register. **(PTU, May 2016 ; Dec. 2012, 2005)**

Ans. 16-bit ring counter with 4-bit shift register.



Initially all the flip-flops are clear.

Thus, FFD, FFC, FFB will be reset or clear but FFA will be preset. Hence, the output of shift register is in the sequence of :

FFD, FFC, FFB and FFA

i.e. $Q_D\ Q_C\ Q_B\ Q_A = 0001$

Negative edge triggered clock is used simultaneously for all the flip-flops.

Case I. Ist negative going clock edge :

Flip flop B will set because, $Q_A = Q_B = 1$

and flip flop A will reset because, $Q_A = Q_C = 0$.

$\therefore$ $Q_D\ Q_C\ Q_B\ Q_A = 0010$

Case II. 2nd negative going clock edge :

Flip flop C will be set because, $Q_C = Q_B = 1$

Also, flip-flop B will reset as $Q_B = Q_A = 0$.

$\therefore$ $Q_D\ Q_C\ Q_B\ Q_A = 0100$.

Similarly, third and fourth clock outputs are :

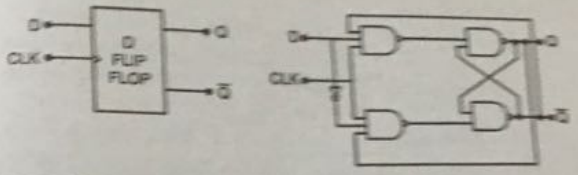
Case III. $Q_D\ Q_C\ Q_B\ Q_A = 1000$

Case IV. $Q_D\ Q_C\ Q_B\ Q_A = 0001$

So, it works as a ring counter.

Q 28. Explain about D flip-flop. (PTU, May 2016 ; Dec. 2006)

Ans. D-Flip-flop : The functional block diagram and internal structure of D flip-flop is as shown :



The D flip-flop has only one input or synchronous control input.

Its truth table is as shown :

Inputs		Output
D	CLK	Q
0	↑	0
1	↑	1

The output Q will go to same state that is present on the D input.

If D = 0, with the passage of clock, Q goes to 0 and if D = 1, the output Q goes to 1 with the passage of clock pulse.

The SR and JK flip-flop can be easily converted to D flip-flop by simple addition of inverter as shown in circuit diagram.

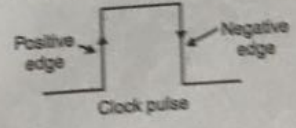
Q 29. Explain Edge triggered flip flop. (PTU, May 2006)

Ans. Edge Triggered Flip-Flop : The flip-flop state is switched by a small change in the input signal. This change is called a trigger and the transition it causes is said to trigger the flip-flop.

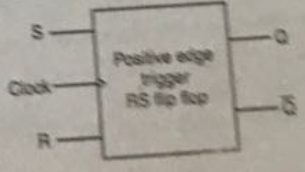
Edge triggered flip-flops are triggered by :

1. Positive edge 2. Negative edge

1. Positive edge triggered flip-flops : In positive edge triggered flip-flops the clock pulse samples the input line at the positive edge or rising edge of the clock pulse.

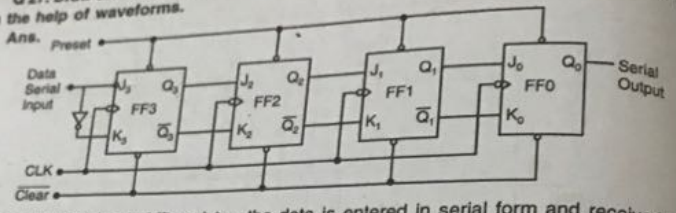


A positive edge triggered flip-flop symbolic representation is as shown :



Q 27. Draw the circuit diagram of a 4 bit serial shift register and explain its working with the help of waveforms. **(PTU, May 2007)**

Ans.



In serial in serial out shift register, the data is entered in serial form and received in serial form. A 4-bit SISO shift register is shown in fig. Assume that we want to store 1010 in the shift register. This will be applied at the input.

Assume register is initially clear. To store 1010, the right most bit '0' is applied at serial input. When negative edge of first clock pulse arrives this '0' is stored into FF3 i.e. output $Q_3 = 0$ also $Q_2 = Q_1 = Q_0 = 0$ already reset.

Now next bit '1' is at serial input making $J_3 = 1$ and $K_3 = 0$. Also $Q_3 = 0$ means $J_2 = 0$ and $\overline{Q}_3 = 1$ means $K_2 = 1$. So when second clock arrives it makes Q_3 and $Q_2 = 0$, also $Q_1 = Q_0 = 0$ already reset.

Similarly, when next bit '0' is at serial input making

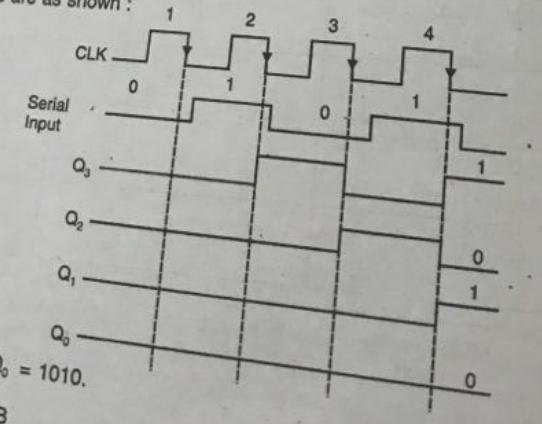
$Q_3 = 1$, $Q_2 = 0$, $Q_1 = 0$, $Q_0 = 1$

$J_3 = 0$, and $K_3 = 1$, thus after clock

$Q_3 = 0$, $Q_2 = 1$, $Q_1 = 0$ and $Q_0 = 0$

Also, when next bit '1' is at serial input, with clock we get, $Q_3 = 1$, $Q_2 = 0$, $Q_1 = 1$ and $Q_0 = 0$

Wave forms are as shown :



$\therefore$ $Q_3\ Q_2\ Q_1\ Q_0 = 1010.$

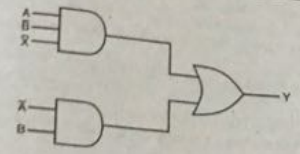
MSB LSB

FF inputs		Output
D_A	D_B	Y
0	0	0
0	1	0
1	1	1
1	0	1
	0	1
	0	0
	1	0
	0	0

$\bar{B}X$	BX	$B\bar{X}$
1	0	1
0	0	1

$= \bar{A}\bar{B}X + B\bar{X}$

For output Y :



Q 33. What is the basic difference between a counter and a shift register?

Ans. **(PTU, May 2009)**

Counter	Shift Register
(i) Counter counts the clock pulses.	(i) Shift register shifts the data left or right.
(ii) Types of counters are : Asynchronous, synchronous, decade, MOD-N, Johnson, ring etc.	(ii) Types of shift registers are : serial in parallel out, serial in serial out, parallel in parallel out, parallel in parallel out, parallel in serial out, bidirectional, universal etc.
(iii) It uses T-flip-flop, J-K flip-flop.	(iii) It uses D-flip flop.
(iv) These are used in banks, railway station etc.	(iv) There are used in memories like RAM, ROM, etc.

Q 34. Explain the difference in operation of a monostable and astable multivibrator.

(PTU, Dec. 2009 ; May 2009)

Ans. Astable multivibrator is a free running multivibrator where as monostable multivibrator is a one shot circuit. Astable generates the square wave form where as monostable is used to generate a gated pulse, whose width can be controlled.

Astable multivibrator has two quasistable states and it does not require any triggering. In case of monostable multivibrator external triggering is required with a pulse of desired duration. It has one stable state and the other as quasi-stable state.

The frequency of astable multivibrator is given by :

$$f = \frac{1}{T} = \frac{1}{1.38RC}$$

where as, the frequency of monostable multivibrator is given by :

$$f = \frac{1}{T} = \frac{1}{0.69RC}$$

The circuit excitation table is as shown :

Present State		Input	Next state		FF inputs		Output
A	B	X	A_{n+1}	B_{n+1}	D_A	D_B	Y
0	0	0	0	0	0	0	0
0	0	1	0	1	0	1	0
0	1	0	1	1	1	1	1
0	1	1	1	0	1	0	1
1	0	0	1	0	1	0	1
1	0	1	0	0	0	0	0
1	1	0	1	1	1	1	0
1	1	1	0	0	0	0	0

K-maps are as shown :

1. For D_A :

A \ BX	$B\bar{X}$	$\bar{B}X$	BX	$B\bar{X}$
$\bar{A}$	0	0	1	1
A	1	0	0	1

$\therefore D_A = \bar{A}B + A\bar{X}$

2. For D_B :

A \ BX	$B\bar{X}$	$\bar{B}X$	BX	$B\bar{X}$
$\bar{A}$	0	1	0	1
A	0	0	0	1

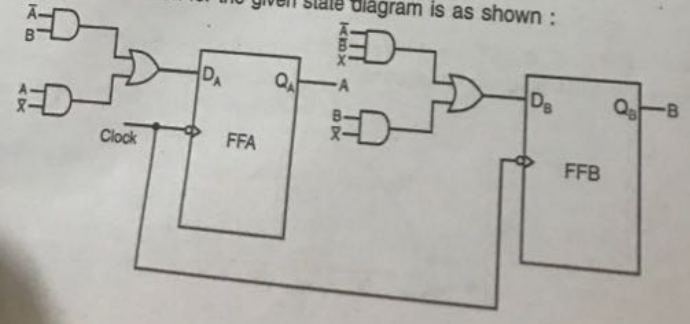
$\therefore D_B = \bar{A}\bar{B}X + B\bar{X}$

3. For Y :

A \ BX	$B\bar{X}$	$\bar{B}X$	BX	$B\bar{X}$
$\bar{A}$	0	0	1	1
A	1	0	0	0

$\therefore Y = A\bar{B}\bar{X} + \bar{A}B$

Circuit implementation for the given state diagram is as shown :

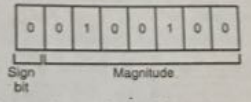


Truth table will clear more :

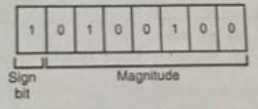
CLK	Q_A	Q_B	Q_C	Q_D
X	1	0	0	0
↓	0	1	0	0
↓	0	0	1	0
↓	0	0	0	1
↓	1	0	0	0

Q 31. Show the contents of an 8 bit register that stores the number +36 and –36 in binary sign magnitude. **(PTU, Dec. 2004)**

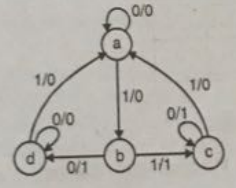
Ans. Contents of an 8-bit register after storing +36 :



Contents of an 8-bit register after storing – 36 :

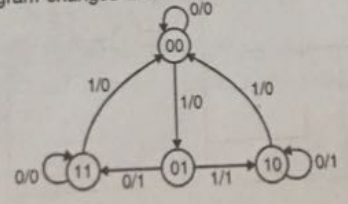


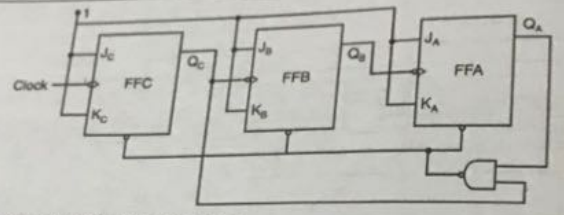
Q 32. Design a circuit that will function according to state diagram given below: **(PTU, Dec. 2009 ; May 2009)**



Ans. Let a = 00, b = 01, c = 10 and d = 11.

Thus, the state diagram changes to :





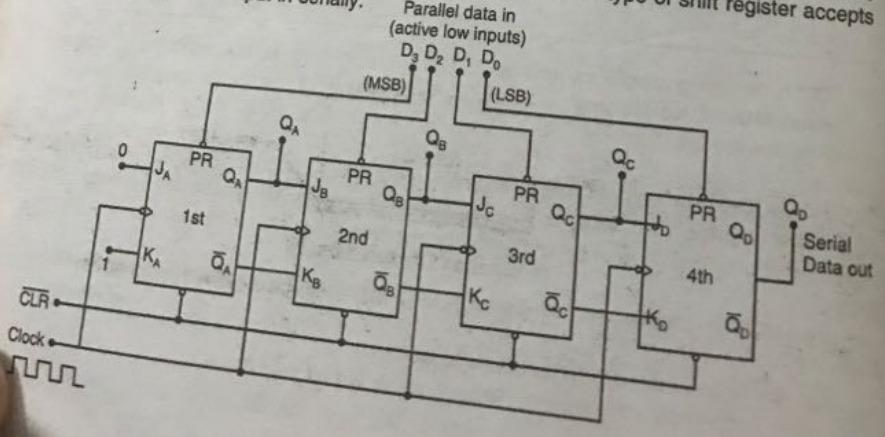
Truth table of MOD-6 up counter is :

Clock	Q_A	Q_B	Q_C	Count
↓	0	0	0	0
↓	0	0	1	1
↓	0	1	0	2
↓	0	1	1	3
↓	1	0	0	4
↓	1	0	1	5
↓	0	0	0	0

After 5th clock it automatically comes to reset state through NAND gate output. Thus, 6 never comes in MOD-6 asynchronous counters.

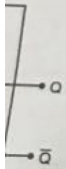
Q 38. Explain how parallel in serial out (PISO) Shift Register works. **(PTU, May 2017 ; Dec. 2008)**

Ans. PISO (Parallel In Series Out) Shift Register : This type of shift register accepts data in parallel and output in serially.



(PTU, Dec. 2011)
ach flip-flop is provided same
rs are triggered at the same

y 2015 ; Dec. 2009, 2008)
may be designed using R-
diagram of master slave JK

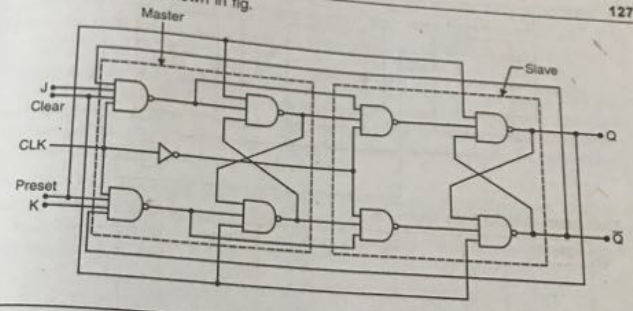


, the CLK_m is 1 and

, the $CLK_m = 0$ and

tion the inputs at J

Truth table is as shown in fig.



Inputs					Outputs	
PR	CLR	CLK	J	K	Q_{n+1}	$\overline{Q}_{n+1}$
0	1	d	d	d	1	0
1	0	d	d	d	0	1
0	0	d	d	d	1	1
1	1	⎍	0	0	No change OR	Hold
1	1	⎍	0	1	0	1
1	1	⎍	1	0	1	0
1	1	⎍	1	1	$\overline{Q}_n$	Q_n

Q 37. Design a mod-6 up counter. **(PTU, May 2017 ; Dec. 2008)**

Ans. MOD-6 up Counter : It can be designed by using either synchronous or asynchronous modes. For simplicity, let us take the designing of MOD-6 up Asynchronous counter.

For MOD-6, number of flip-flops required are :

If the counting of counter is known, we can calculate the number of flip-flops. The largest number which counter counts gives the number of flip-flops after calculating its binary form.

The MOD-N counter will count upto N – 1 i.e. for MOD-6 counter the counting is upto 6 – 1 = 5.

So, the largest count is 5. Its binary is $(101)_2$.

Thus, 3 flip-flops are required. Since, numbers of binary bits are 3.

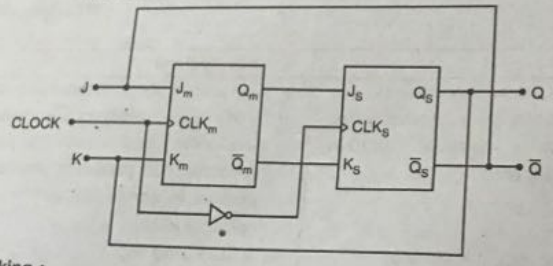
Q 35. What are synchronous counters? **(PTU, Dec. 2011)**

Ans. *Synchronous counters are those counters in which each flip-flop is provided same clock pulse. Thus all the flip-flops used in synchronous counters are triggered at the same time.*

Q 36. Explain the working of master slave JK flip-flop. **(PTU, May 2015 ; Dec. 2009, 2008)**

Ans. Master slave JK flip-flop : *The master slave flip-flop may be designed using R-S, D and JK flip-flops. Following figure shows the functional block diagram of master slave JK flip-flop :*

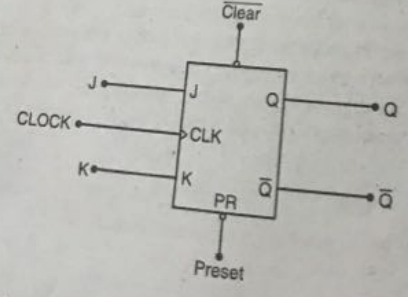
In figure m is used for Master and
S is used for Slave



Working :

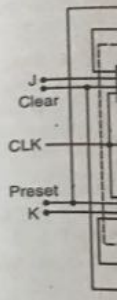
Case 1 : *When positive clock pulse goes on, leading edge is applied, the CLK_m is 1 and CLK_s is 0, then data transferred to Q_m is held upto CLK = 1.*

Case 2 : *When the clock pulse goes negative, trailing edge is applied, the $CLK_m = 0$ and $CLK_s = 1$, then Q_m and $\overline{Q}_m$ will be transferred to $Q = \overline{Q}$ and at that duration the inputs at J and K should not change. This is overcome by the use of data lockout.*



Internal structures of master slave J-K flip-flop.

Truth table



PR
0
1
0
1
1
1
1

Q 37. De

Ans. MO

asynchronous
counter.

For MOD

If the co
largest numbe
form.

The MO
6 – 1 = 5.

So, the
Thus, 3

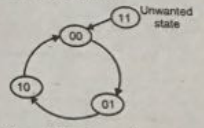
At last we get $Q_3\,Q_2\,Q_1\,Q_0 = 0000$
It is clearly shown in timing waveforms.

Q 41. Design a MOD-3 synchronous counter using J-K Flip-Flops. **(PTU, May 2017, 2008)**

Ans. MOD-3 synchronous counter using J-K flip-flops.
Truth table is as shown :

Q_B	Q_A
0	0
0	1
1	0

State Diagram :



The number of flip flops required are : 2. It is a MOD-3 synchronous counters since the numbers of states is 3.

Excitation Table of J-K flip-flop is as shown :

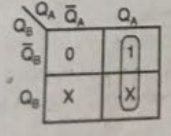
Present State Q_n	Next State Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Thus, the circuit excitation table is as shown :

Present State		Next State		Flip flop Inputs			
Q_B	Q_A	Q_{B+1}	Q_{A+1}	J_B	K_B	J_A	K_A
0	0	0	1	0	X	1	X
0	1	1	0	1	X	X	1
1	0	0	0	X	1	0	X
1	1	0	0	X	1	X	1

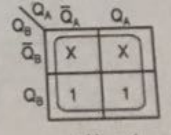
K-maps and simplification are as shown :

For J_B :



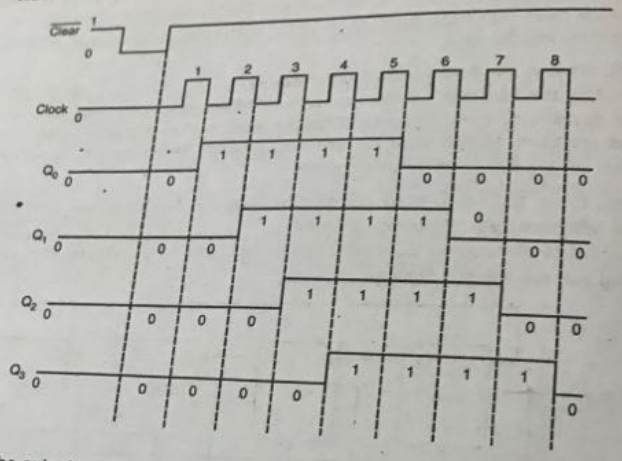
$\therefore J_B = Q_A$

For K_B :



$\therefore K_B = 1$

Waveform are as shown :



Initially the outputs of flip flops are :

$Q_3 Q_2 Q_1 Q_0 = 0000$

As $\overline{Q_3} = 1$, thus $D_0 = 1$

⇒ At Ist falling edge of clock pulse :

The output changes to :

$Q_3 Q_2 Q_1 Q_0 = 0001$

⇒ At 2nd falling edge of clock pulse :

The output changes to :

$Q_3 Q_2 Q_1 Q_0 = 0011$

⇒ At 3rd falling edge of clock pulse :

The output changes to :

$Q_3 Q_2 Q_1 Q_0 = 0111$

⇒ At 4th clock pulse :

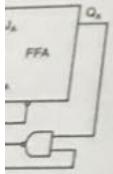
The outputs are :

$Q_3 Q_2 Q_1 Q_0 = 1111$

⇒ At 5th clock pulse :

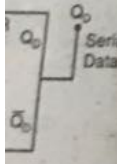
The outputs are :

$Q_3 Q_2 Q_1 Q_0 = 1110$



gate output. Thus, 6

works.
2017 ; Dec. 2008)
hift register accepts



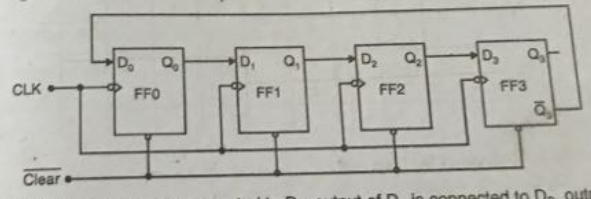
Working : The data low input sets the flip-flops forcefully as data is given to preset pin. Let 1010 is parallel data in. It is active low pin. Thus, gives 0101 to the $\overline{PR}$ pins of all flip-flop. Which gives output $Q_A\ Q_B\ Q_C\ Q_D$ = 1010, when clock pulse occur. It shifts the data right and serially out the data.

Q 39. What is the function of multivibrator? **(PTU, May 2012)**

Ans. Almost all the digital system required timing waveforms. For example : all clocked sequential system requires a source of trigger pulse and in digital systems rectangular waveforms are used. Multivibrator function is to produce timing waveforms in the form of rectangular, square etc. for the digital system.

Q 40. Draw the logic diagram of 4-bit Twisted Ring counter and explain its operation with the help of timing diagram. **(PTU, May 2017, 2008)**

Ans. Twiste ring counter is known as Johnson counter. Following figure shows the 4-bit twisted ring counter using D flip-flops :



When the output of D_0 is connected to D_1, output of D_1 is connected to D_2, output of D_2 is connected to D_3 and output $\overline{Q}_3$ of D_3 is connected to D_0 then the counter is known as Johnson or twisted ring counter for 4-bits.

Its truth table is as shown :

Clock	$\overline{Clear}$	Q_0	Q_1	Q_2	Q_3
⎍	⎍	1	0	0	0
↓	1	1	1	0	0
↓	1	1	1	1	0
↓	1	1	1	1	1
↓	1	0	1	1	1
↓	1	0	0	1	1
↓	1	0	0	0	1
↓	1	0	0	0	0
↓	1	1	0	0	0

For stable table :
Present state AB = 00
⇒ Next state with XY = 00

1. $J_A = BX + \overline{B}\,\overline{Y}$ and $K_A = \overline{B}X\overline{Y}$

$\therefore J_A = 0 + 1 = 1$ and $K_A = 1.0.1 = 0$

Output :

$$Z = AXY + B\overline{X}\,\overline{Y}$$

$$= 0.0.0 + 0.\overline{0}.\overline{0}$$

$$\therefore Z = 0$$

2. $J_B = \overline{A}X = 1.0$ and $K_B = A + X\overline{Y}$

$\therefore J_B = 0$ and $K_B = 0 + (0.1) = 0$

Thus, $A_{n+1} = 1$ as FFA is set and $B_{n+1} = 0$ as there is no change in the FFB status.

Therefore, next state = 10 and output Z = 0.

⇒ Next state with XY = 01

$J_A = 0, K_A = 0 \therefore A_{n+1} = A = 0$ output Z = 0

$J_B = 0, K_B = 0 \therefore B_{n+1} = B = 0 \therefore$ Next state = 00.

⇒ Next state with XY = 10

$J_A = 1, K_A = 1 \quad \therefore A_{n+1} = \overline{A} = 1$

$J_B = 1, K_B = 1 \quad \therefore B_{n+1} = \overline{B} = 1$

output $Z = AXY + B\overline{X}\,\overline{Y}$

$= (0.1.0) + \left(0.\overline{1}.\overline{0}\right)$

$\therefore Z = 0$

$\therefore$ Next state = 11.

Next state with XY = 11

$J_A = 0, K_A = 0 \quad \therefore A_{n+1} = A = 0$

$J_B = 1, K_B = 0 \quad \therefore B_{n+1} = 1$

output $Z = AXY + B\overline{X}\,\overline{Y}$

$= (0.1.1) + \left(0.\overline{1}.\overline{1}\right)$

$\therefore Z = 0$

$\therefore$ Next state = 01.

Thus, the state table is given as :

Present state		Next state/Output Z			
A	B	XY = 00	XY = 01	XY = 10	XY = 11
0	0	10/0	00/0	11/0	01/0
0	1	01/1	01/1	10/1	11/0
1	0	10/0	10/0	00/0	10/1
1	1	10/1	10/1	10/1	10/1

K_A :

$Q_A\ \bar{Q}_A$	Q_A
X	1
X	1

$\therefore K_A = 1$

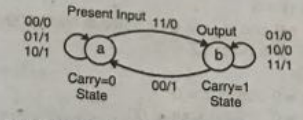
p-flops.

owing sequential circuit.
S (PTU, Dec. 2007)

Consider a = 0 state and b = 1 state. Thus, the state table is given as :

Present state (y_1)	Input xy	Next state	Output Y	State Name
0	0 0	0	0	a
0	0 1	0	1	a
0	1 0	1	0	b
0	1 1	0	1	a
1	0 0	0	1	a
1	0 1	1	0	b
1	1 0	1	1	b
1	1 1	1	0	b

The state diagram is as follows :

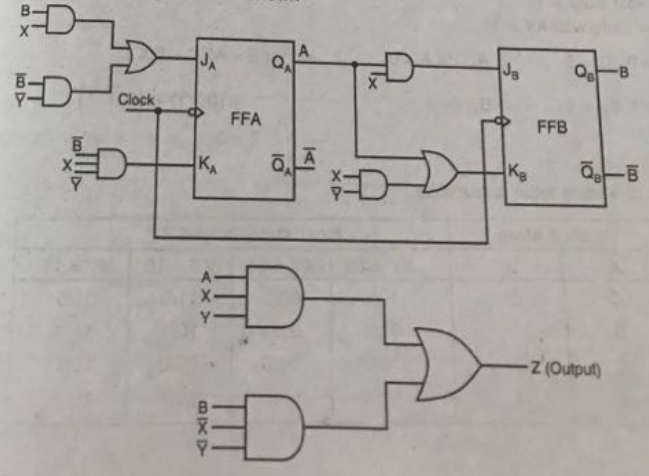


Q 43. A sequential circuit has two JK flip flop A and B, two input X and Y and one output Z. The flip flop input equations and output functions are as follows :

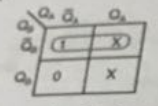
$J_A = BX + \bar{B}\bar{Y}$, $K_A = \bar{B}XY$, $Z = AX\bar{Y} + B\bar{X}\bar{Y}$, $J_B = \bar{A}X$ and $K_B = A + X\bar{Y}$.

Draw the logic diagram of the circuit. Also derive the state table and state diagram of the circuit. (PTU, May 2007)

Ans. The logic diagram is as shown

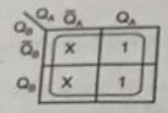


For J_A :



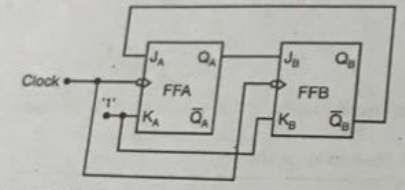
$\therefore J_A = \bar{Q}_B$

For K_A :



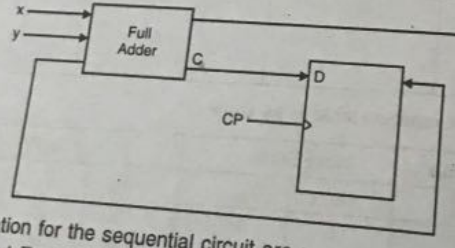
$\therefore K_A = 1$

Implementation of logic diagram is as shown :



Logic diagram of MOD-3 synchronous counter using J-K flip-flops.

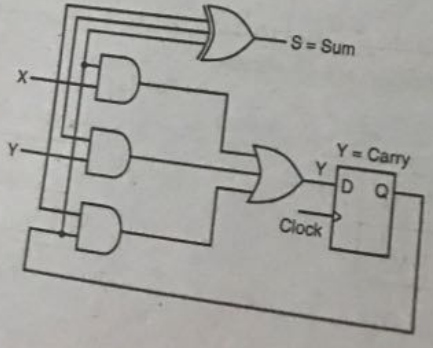
Q 42. Derive the state table and state diagram of the following sequential circuit. (PTU, Dec. 2007)



Ans. The equation for the sequential circuit are :

Output $Z = x \oplus y \oplus y_1$

$Y = xy + xy_1 + yy_1$

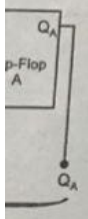


ister. (PTU, Dec. 2013)
r simultaneously data is
is parallel input data will

e same data as applied

ollected in parallel form

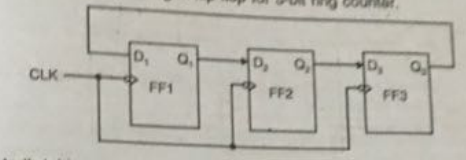
p. Thus data will be at
ll be 0101 then output



(PTU, Dec. 2009)
atever we provide

Q 47. What is a ring counter? (PTU, Dec. 2015, 2012, 2009)

Ans. Ring counter is the counter in which output of last stage is feedback to input of first stage. It is as shown in fig. using D flip-flop for 3-bit ring counter.



The truth table is as shown

	Q_1	Q_2	Q_3	CLK Pulse
Reference State	1	0	0	
	0	1	0	1
	0	0	1	2
	1	0	0	3

Q 48. What is significance of figure of merit of flip flops? (PTU, May 2010)

Ans. The minimum clock period at which a circuit can work depends upon the clock to Q delay and setup time of flip-flop. The figure of merit for a flip-flop is the sum of clock to delay of flip-flop and setup line i.e. $T_{CP} + T_{SU}$.

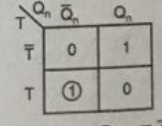
Q 49. Convert a D flip flop into a T flip flop. (PTU, May 2010)

Ans. Conversion of 'D' flip-flop to 'T' flip-flop :

The truth table for D to T flip-flop is given by

Inputs			Output
T	Present State Q_n	Next State Q_{n+1}	D
0	0	0	0
1	0	1	1
1	1	0	0
0	1	1	1

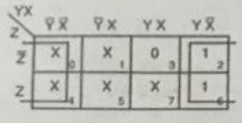
K-map for D is as shown :



$$\therefore \quad D = T\bar{Q}_n + \bar{T}Q_n$$

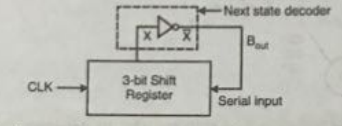
$$= T \oplus Q_n$$

K-map :



$\therefore B_{out} = \bar{X}$

The logic diagram is as shown :



Q 45. Explain the working of parallel-in-parallel-out shift register. (PTU, Dec. 2013)

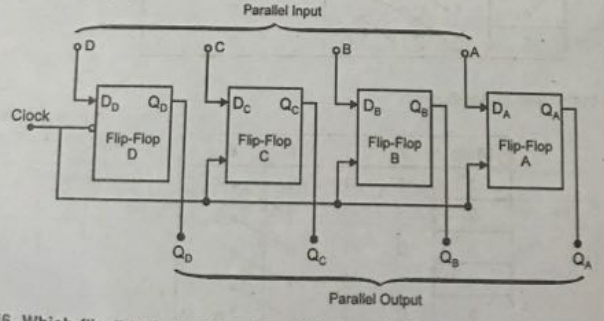
Ans. It is in short known as PIPO shift register. In this register simultaneously data is entered from parallel inputs and with the application of clock pulse this parallel input data will be at the output of corresponding flip-flop.

For PIPO shift register D-flip flop is used because it will store the same data as applied at the input.

Whenever clock pulse is given the input data is stored will be collected in parallel form simultaneously as shown in fig.

In fig. A, B, C, D connected to the input data pin of each D flip-flop. Thus data will be at D_A D_B D_C D_D parallel data output line will be $Q_AQ_BQ_CQ_D$. So if input will be 0101 then output will be

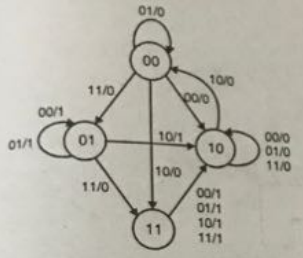
$$Q_AQ_BQ_CQ_D = 0101$$



Q 46. Which flip flop is preferred for data transfer? (PTU, Dec. 2009)

Ans. D flip-flop is preferred for data transfer. Because in D flip-flop whatever we provide at the input will be stored in the flip-flop with the passage of clock.

Now, the state diagram is as shown from the state table given above :



Input XY = 01
Output Z = 0
Present state = 00.

FFB status.

Q 44. Design and draw the circuit of shift register to generate the following wave train ..... 1101011 ..... (PTU, Dec. 2005, 2004)

Ans. As the sequence is :

1 1 0 1 0 1 1

It repeats after 5 bits i.e. 11010 so 3-flip-flops are required.

Table shows the state table for it :

State	Z	Y	X	Equivalent Decimel
1	1	1	0	6
2	1	0	1	5
3	0	1	0	2
4	1	0	1	5
5	0	1	1	3

The truth table to get B_{out} is :

State	Z	Y	X	B_{out}
1	1	1	0	1
2	1	0	1	0
3	0	1	0	1
4	1	0	1	1
5	0	1	1	0

Fig. 2 shows the general diagram of multivibrator from which all multivibrators can derive.

As stable multivibrator uses two capacitors in each feedback loop i.e. $F_1 = C_1$ and $F_2 = C_2$. It is as shown in fig. 3.

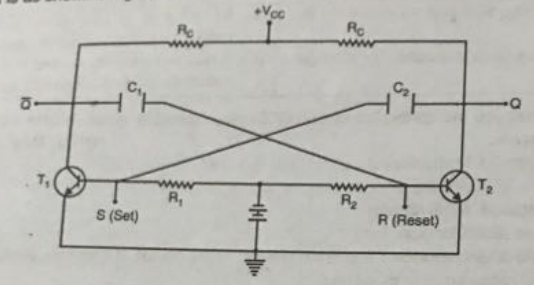


Fig. 3. Astable Multivibrator

Working : Let us assume T_1 is ON and T_2 is OFF i.e. T_1 is in saturation state and cross coupled to T_2. If $Q = 1$, then $\overline{Q} = 0$ it remains same untill triggered externally by pulse at S or R.

To change the states provide negative pulse to R and positive pulse to S. Then Q becomes '0' and $\overline{Q} = 1$, as T_1 will be OFF and T_2 will be ON.

Q 53. How many pulses are needed to change the contents of a 8 bit up-counter from 10101100 to 00100111? **(PTU, Dec. 2011)**

Ans. $(10101100)_2 = (172)_{10}$

$(00100111)_2 = (39)_{10}$

Also, $(11111111)_2 = (255)_{10}$

Number of pulses to change the contents of a 8 bit up counter from (10101100) to (00100111) can be calculated by taken 1's complement of larger number and add it to smaller number. It is as shown :

$$\begin{array}{l} (10101100) \leftarrow \text{larger number} \\ (01010011) \leftarrow \text{1's complement of larger number} \\ +\ (00100111) \\ \hline (01111010)_2 \\ \hline \end{array}$$

$\therefore \quad (01111010)_2 = (122)_{10}$

Thus, 122 pulses are required to change the contents of a 8-bit up-counter for given data.

Q 51. Explain the difference between the following : S-R flip flop and Bistable multivibrator. **(PTU, Dec. 2010)**

Ans. S-R flip flop and Bistable multivibrator.

S-R Flip Flop	Bistable Multivibrator
(a) S-R flip flop is called as set-reset flip flop.	(a) Because of its two stable states it is called as bistable multivibrator.
(b) It does not uses capacitor for storage.	(b) It has two capacitors used in shunt with resistors for fast triggering speed.

Q 52. What are multivibrator circuits? Explain Astable multivibrator with the help of circuit diagram. **(PTU, May 2012, 2010)**

Ans. Types of Multivibrator :

1. Astable Multivibrator
2. Monostrable Multivibrator
3. Bistable Multivibrator

1. Astable Multivibrator : It is free running multivibrator. It has two quasistable states which does not required any triggering.

Example of Astable Multivibrator : The inverter with feedback is an example of astable multivibrator as shown i.e. fig. 1.

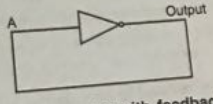


Fig. 1 Inverter with feedback

When A = 0, output = 1 and that is given as A = 1, output = 0 i.e. output is oscillating and no stable output.

Fig. 2 shows the general block diagram of multivibrator.

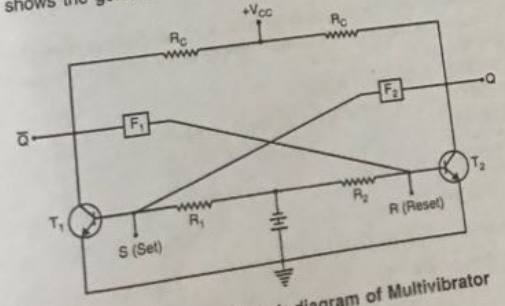
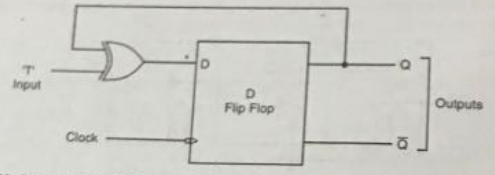


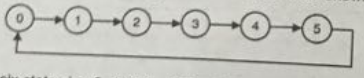
Fig. 2 General block diagram of Multivibrator

The conversion of D flip-flop to T flip-flop is as shown :



Q 50. Design a MOD 6 counter using T-flip flops. **(PTU, May 2010)**

Ans. State diagram of MOD-6 asychronous counter is as shown :

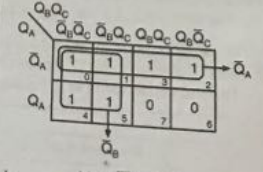


It will count six states i.e. 0, 1, 2, 3, 4, 5 and then reset to 0.

Truth table of MOD-6 asynchronous counter is as shown.

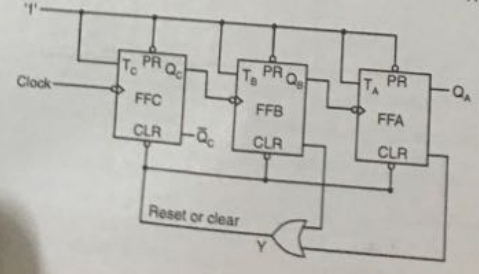
Flip Flop outputs			Output clear for reset
Q_A	Q_B	Q_C	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

The K-map for clear logic is given by :

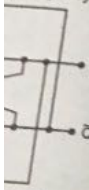


$\therefore$ $Y = \overline{Q}_A + \overline{Q}_B$

Implementation :



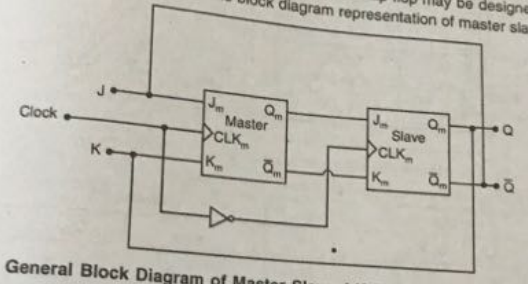
Master Slave Flip
7, 2016, 2014, 2010)
in J-K latch, when
lled by enable (EN)
ith logic symbol.



lip-flop
thus change in
J = K = 1, the
s is called the
l be uncertain
ere is a race
ear from the

The race-around condition can be avoided if enable signal is reduced than propagation delay of flip-flop i.e., $t < t_p < T$, (as shown in the previous waveforms) but it is not practically feasible. Thus, master-slave flip-flop is used.

Master Slave J-K Flip-Flop : The master slave flip-flop may be designed using R – S, D and J-K flip-flops. Fig. shows the block diagram representation of master slave J-K flip-flop.



General Block Diagram of Master Slave J-K flip-flop having NAND gates

Working :

Case 1. When positive clock pulse goes on, leading edge is applied, the $CLK_m = 1$ and $CLKs = 0$, then data transferred to Q_m is hold here upto CLK = 1.

Case 2. When the clock pulse goes negative, trailing edge is applied, the $CLK_m = 0$ and $CLKs = 1$, then Q_m and $\overline{Q}_m$ will be transferred to Q and $\overline{Q}$ and at that duration the inputs at J and K should not change. This is overcome by the use of data lockout.

The symbol and full circuitry is shown in fig. (a) and Fig. (b).

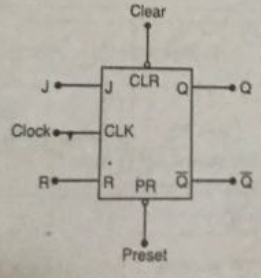
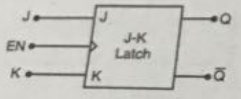


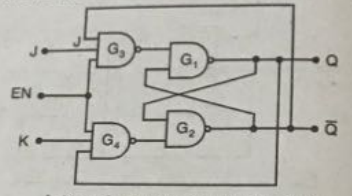
Fig. (a) Symbol

Q 55. What is race around condition? How it is avoided in Master Slave Flip Flop? **(PTU, May 2014, 2013, 2012, 2011 ; Dec. 2017, 2016, 2014, 2010)**

Ans. Race Around Condition : Race around condition occurs in J-K latch, when J = K = 1 i.e., when the J-K latch is in toggle state. Latches are controlled by enable (EN) signal and are level triggered. Following fig. shows the J-K latch circuit with logic symbol.

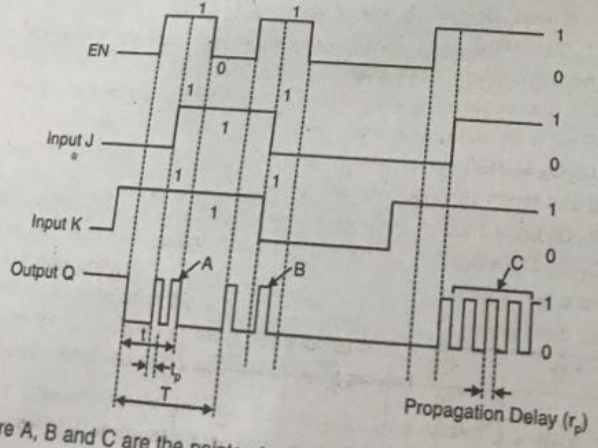


Logic symbol



Internal structure J-K flip-flop

This J-K latch circuit is not practical. The output is feedback to input and thus change in output results in input change. During positive half cycle of clock pulse, when J = K = 1, the output keep on changing from 0 to 1, then 1 to 0, then 0 to 1 and so on. This is called the toggle state. The output toggles continuously and at the end of pulse its state will be uncertain i.e., whether '0' comes first or '1' comes first at the output we don't know. There is a race between '0' and '1'. This condition is called as race around condition. It is clear from the waveforms as shown :

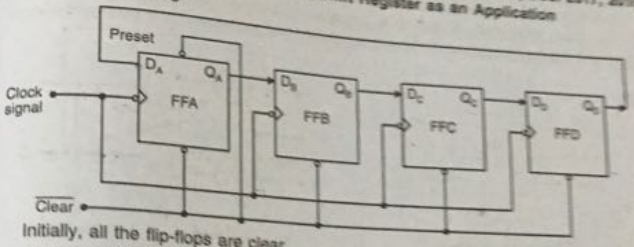


Here A, B and C are the points showing the continuous toggling of output when, inputs = 1 and K = 1 during the enable (En) = 1. When EN = 0, there is no change condition we get the previous output for Low enable signal. Also, the output transition occurs after propagation delay time.

Q 54. Draw the circuit of a 4 bit ring counter with negative edge triggered J-K flip flops and explain its operation with timing diagrams. (PTU, Dec. 2017, 2010)

Ans. 4-Bit Ring Counter With 4-Bit Shift Register as an Application

It is as shown in fig.



Initially, all the flip-flops are clear.

Thus, FFD , FFC, FFB will be reset or clear but FFA will be preset. Hence, the output of shift register is in the sequence of FFD, FFC, FFB and FFA

i.e. $Q_D\, Q_C\, Q_B\, Q_A = 0001$

Negative edge triggered clock is used simultaneously for all the flip-flops.

Case I. Ist negative going clock edge

Flip-flop B will set because, $Q_A = Q_B = 1$

and flip-flop A will reset because, $Q_A = Q_C = 0$.

$\therefore \quad Q_D\, Q_C\, Q_B\, Q_A = 0010$

Case II. 2nd negative going clock edge

Flip-flop C will be set because, $Q_C = Q_B = 1$

Also, flip-flop B will reset as $Q_B = Q_A = 0$.

$\therefore \quad Q_D\, Q_C\, Q_B\, Q_A = 0100$.

Similarly, third and fourth clock outputs are

Case III. $Q_D\, Q_C\, Q_B\, Q_A = 1000$

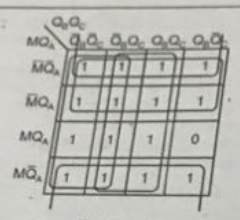
Case IV. $Q_D\, Q_C\, Q_B\, Q_A = 0001$

So, it works as a ring counter.

Truth table will clear more

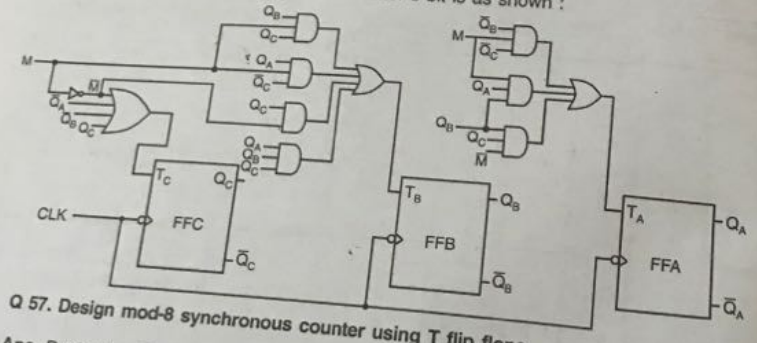
CLK	Q_A	Q_B	Q_C	Q_D
X	1	0	0	0
↓	0	1	0	0
↓	0	0	1	0
↓	0	0	0	1
↓	1	0	0	0

For T_C :



$\therefore \quad T_C = \bar{M} + \bar{Q}_A + \bar{Q}_B + Q_C$

- Implementation of MOD 6 up-down counter 3 bit is as shown :



Q 57. Design mod-8 synchronous counter using T flip flops. **(PTU, Dec. 2016 ; May 2012, 2011)**

Ans. Designing of MOD-8 synchronous counter using T flip-flops.

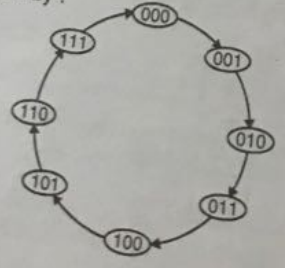
Number of flip-flops required are given by :

$$N \leq 2^n$$

Here, $N = 8 \therefore 8 \leq 2^3 \quad (\because 2^3 = 8)$

Thus, it has 8 states i.e. 000, 001, 010, 011, 100, 101, 110, 111 and after that it again resets to 000 and so on. So it requires 3 flip flops.

Its state diagram is given by :



for appropriate period of time and at that time the output will enable the latch. That circuit is called as pulse detector. It is as shown in fig. (a) and the waveforms are shown in fig. (b).

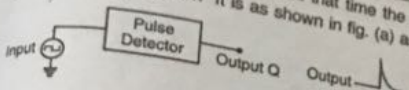


Fig. (a) Pulse Detector with input and output

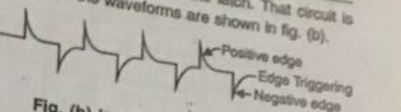


Fig. (b) Input and Output waveforms for Pulse Detector

Q 56. Design a three bit, MOD 6, unit distance up-down counter. (PTU, May 2010)

Ans. 3-bit MOD-6 counter has 3 flip-flops which toggles. Let up counting takes place for mode control M = 0 and down counting takes place for mode control M = 1.

The excitation table for 3-bit MOD-6 synchronous counter is as shown :

Mode Control	Present State			Next State			Inputs to flip-flops		
M	Q_A	Q_B	Q_C	Q_{A+1}	Q_{B+1}	Q_{C+1}	T_A	T_B	T_C
0	0	0	0	0	0	1	0	0	1
0	0	0	1	0	1	0	0	1	1
0	0	1	0	0	1	1	0	0	1
0	0	1	1	1	0	0	1	1	1
0	1	0	0	1	0	1	0	0	1
0	1	0	1	1	1	0	0	1	1
0	1	1	0	0	0	0	0	1	1
0	1	1	1	0	0	0	0	0	1
1	0	0	0	1	0	1	1	0	1
1	0	0	1	0	0	0	0	0	1
1	0	1	0	0	0	1	0	1	1
1	0	1	1	0	1	0	0	0	1
1	1	0	0	0	1	1	1	1	1
1	1	0	1	1	0	0	0	0	1
1	1	1	0	0	0	0	1	1	0
1	1	1	1	0	0	0	1	1	1

K-map :

For T_A :

MQ_A \ Q_BQ_C	$\bar{Q}_B\bar{Q}_C$	$\bar{Q}_BQ_C$	Q_BQ_C	$Q_B\bar{Q}_C$
$\bar{M}\bar{Q}_A$	0	0	1	0
$\bar{M}Q_A$	0	0	1	0
MQ_A	1	0	1	1
$M\bar{Q}_A$	1	0	0	0

$\therefore T_A = M\bar{Q}_B\bar{Q}_C + MQ_AQ_B + \bar{M}Q_BQ_C$

For T_B :

MQ_A \ Q_BQ_C	$\bar{Q}_B\bar{Q}_C$	$\bar{Q}_BQ_C$	Q_BQ_C	$Q_B\bar{Q}_C$
$\bar{M}\bar{Q}_A$	0	1	1	0
$\bar{M}Q_A$	0	1	1	0
MQ_A	1	0	1	1
$M\bar{Q}_A$	0	0	0	1

$\therefore T_B = M\bar{Q}_C + MQ_A\bar{Q}_C + Q_AQ_BQ_C + MQ_B\bar{Q}_C$

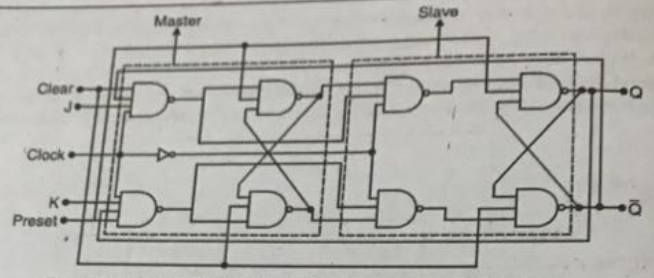
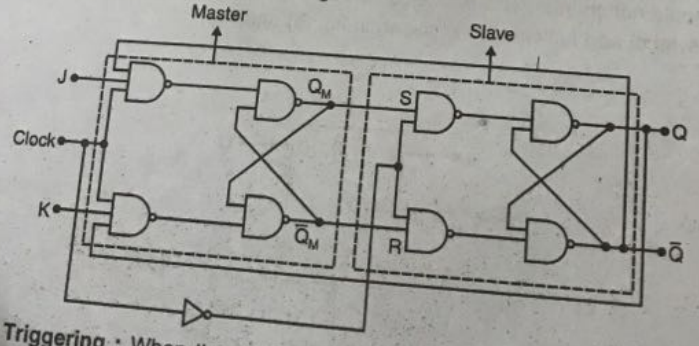


Fig. (b) Internal Structure of Master Slave J-K Flip-Flop

The truth table is shown where 'd' and don't care conditions.

Inputs					Outputs	
PR	CLR	CLK	J	K	Q_{n+1}	$\bar{Q}_{n+1}$
0	1	d	d	d	1	0
-1	0	d	d	d	0	1
0	0	d	d	d	1	1
1	1	⊓(1)	0	0	No change	or Hold
1	1	⊓(1)	0	1	0	1
1	1	⊓(1)	1	0	1	0
1	1	⊓(1)	1	1	$\bar{Q}_n$	Q_n

It may also be drawn as shown in fig.



Edge Triggering : When the clock input (level or edge triggered) is provided to S-R latch, then it is called as S-R flip-flop. S-R latch responds for inputs (S and R) only for the enabled input.

In gated S-R latch NAND gates coupled with S-R latch, but in edge triggering (falling and rising) there is a digital circuit required that gives output of brief pulses whenever input is occur

Q 59. Design a T-flip-flop counter that goes through the states 0, 2, 4, 6, 0, 2 ....

Ans. States are (0, 2, 4, 6)

Decimal Equivalent	Present State			Next State			Flip-flop Inputs		
	Q_C	Q_B	Q_A	Q'_C	Q'_B	Q'_A	T_C	T_B	T_A
0	0	0	0	0	1	0	0	1	0
1	0	0	1	0	0	0	0	0	1
2	0	1	0	1	0	0	1	1	0
3	0	1	1	0	0	0	0	1	1
4	1	0	0	1	1	0	0	1	0
5	1	0	1	0	0	0	1	0	1
6	1	1	0	0	0	0	1	1	0
7	1	1	1	0	0	0	1	1	1

K-maps are shown below :

For $T_C \rightarrow$

Q_C \ Q_BQ_A	$\bar{Q}_B\bar{Q}_A$	$\bar{Q}_BQ_A$	Q_BQ_A	$Q_B\bar{Q}_A$
$\bar{Q}_C$	0	0	0	1
Q_C	0	1	1	1

$\therefore T_C = Q_B\bar{Q}_A + Q_AQ_C$

For $T_B \rightarrow$

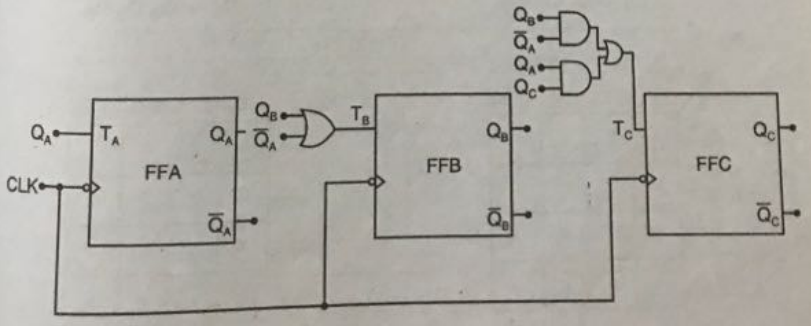
Q_C \ Q_BQ_A	$\bar{Q}_B\bar{Q}_A$	$\bar{Q}_BQ_A$	Q_BQ_A	$Q_B\bar{Q}_A$
$\bar{Q}_C$	1	0	1	1
Q_C	1	0	1	1

$\therefore T_B = Q_B + \bar{Q}_A$

For $T_A \rightarrow$

Q_C \ Q_BQ_A	$\bar{Q}_B\bar{Q}_A$	$\bar{Q}_BQ_A$	Q_BQ_A	$Q_B\bar{Q}_A$
$\bar{Q}_C$	0	1	1	0
Q_C	0	1	1	0

$\therefore T_A = Q_A$



Decimal Equivalent	Present State			Next State			Flip-flop Inputs					
	Q_C	Q_B	Q_A	Q'_C	Q'_B	Q'_A	J_C	K_C	J_B	K_B	J_A	K_A
0	0	0	0	0	0	1	0	X	0	X	1	X
1	0	0	1	0	1	1	0	X	1	X	X	0
2	0	1	0	0	0	1	0	X	X	1	1	X
3	0	1	1	1	0	1	1	X	X	1	X	0
4	1	0	0	0	0	1	X	1	0	X	1	X
5	1	0	1	1	1	1	X	0	1	X	X	0
6	1	1	0	0	0	1	X	1	X	1	1	X
7	1	1	1	0	0	1	X	1	X	1	X	0

K-maps are shown below :

For $J_C \rightarrow$

Q_C \ Q_BQ_A	$\bar{Q}_B\bar{Q}_A$	$\bar{Q}_BQ_A$	Q_BQ_A	$Q_B\bar{Q}_A$
$\bar{Q}_C$	0	0	1	0
Q_C	X	X	X	X

$\therefore J_C = Q_BQ_A$

For $K_C \rightarrow$a

Q_C \ Q_BQ_A	$\bar{Q}_B\bar{Q}_A$	$\bar{Q}_BQ_A$	Q_BQ_A	$Q_B\bar{Q}_A$
$\bar{Q}_C$	X	X	X	X
Q_C	1	0	1	1

$\therefore K_C = Q_B + \bar{Q}_A$

For $J_B \rightarrow$

Q_C \ Q_BQ_A	$\bar{Q}_B\bar{Q}_A$	$\bar{Q}_BQ_A$	Q_BQ_A	$Q_B\bar{Q}_A$
$\bar{Q}_C$	0	1	X	X
Q_C	0	1	X	X

$\therefore J_B = Q_A$

For $K_B \rightarrow$

Q_C \ Q_BQ_A	$\bar{Q}_B\bar{Q}_A$	$\bar{Q}_BQ_A$	Q_BQ_A	$Q_B\bar{Q}_A$
$\bar{Q}_C$	X	X	1	1
Q_C	X	X	1	1

$\therefore K_B = 1$

For $J_A \rightarrow$

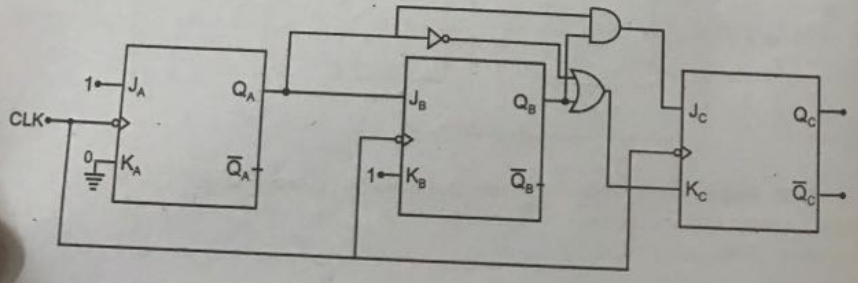
Q_C \ Q_BQ_A	$\bar{Q}_B\bar{Q}_A$	$\bar{Q}_BQ_A$	Q_BQ_A	$Q_B\bar{Q}_A$
$\bar{Q}_C$	1	X	X	1
Q_C	1	X	X	1

$\therefore J_A = 1$

For $K_A \rightarrow$

Q_C \ Q_BQ_A	$\bar{Q}_B\bar{Q}_A$	$\bar{Q}_BQ_A$	Q_BQ_A	$Q_B\bar{Q}_A$
$\bar{Q}_C$	X	0	0	X
Q_C	X	0	0	X

$\therefore K_A = 0$

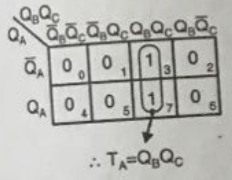


e truth table (or) state table for MOD-8 synchronous counter using T-flip flops in :

Present States		Next States			Required Excitations		
Q_B	Q_C	Q_{A+1}	Q_{B+1}	Q_{C+1}	T_A	T_B	T_C
0	0	0	0	1	0	0	1
0	1	0	1	0	0	1	1
1	0	0	1	1	0	0	1
1	1	1	0	0	1	1	1
0	0	1	0	1	0	0	1
0	1	1	1	0	0	1	1
1	0	1	1	1	0	0	1
1	1	0	0	0	1	1	1

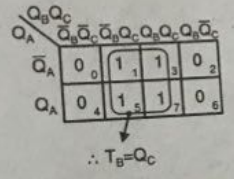
For minimal expression the K-maps are as shown :

For T_A



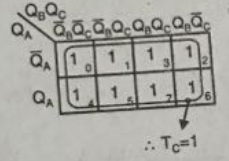
$\therefore T_A = Q_BQ_C$

For T_B



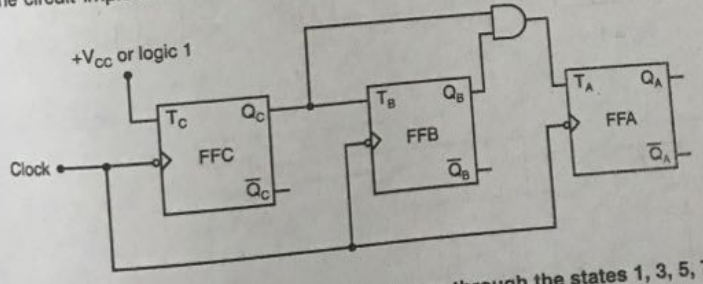
$\therefore T_B = Q_C$

For T_C



$\therefore T_C = 1$

The circuit implementation is as shown in fig.



Q 58. Design a J-K flip-flop counter that goes through the states 1, 3, 5, 7, 1, 3, ... is the counter self correcting.

Ans. States are (1, 3, 5, 7)

The initial data in the controlled buffer register is reset to '0' by applying 'low' signal at the $\overline{\text{Clear}}$ or $\overline{\text{reset}}$ input. Thus, we get the data in all the flip-flop is

$$Q_D Q_C Q_B Q_A = 0000$$

The controlled buffer register is now provided by an 'high' signal through the clear or reset pin of register. Now the register is ready to perform for action.

Case I. When load input is high, the gates G_1, G_2, G_3 and G_4 are activated and the data D_3, D_2, D_1 and D_0 is loaded into the flip-flops through inputs D_D, D_C, D_B and D_A of respective flip-flops at the positive-edge of next clock pulse.

Thus, we get the data in all the flip-flops as

$$Q_D\, Q_C\, Q_B\, Q_A = D_3\, D_2\, D_1\, D_0$$

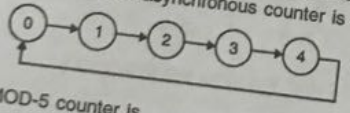
Case II. When load input is 'low', the gates G_1, G_2, G_3 and G_4 are disabled and gates G_5, G_6, G_7 and G_8 are activated. Thus, the data output of corresponding flip-flops are feedback to its respective inputs.

Thus, data is controlled by control input 'load' to retained as each clock pulse is provided. Thus, the contents of controlled buffer register remains unchanged inspite of application of clock pulses. If number of flip-flops are increased, controlled buffer register with larger number of bits can be designed.

Q 64. Draw a logic diagram and waveform for mod – 5 counter.

Ans. Design MOD-5 Asychronous or Ripple Counter **(PTU, May 2013 ; Dec. 2011)**

The state diagram for MOD-5 asynchronous counter is as shown



Truth table of MOD-5 counter is

States	Flip-Flop Outputs			Clear
	Q_C	Q_B	Q_A	
0	0	0	0	1
1	0	0	1	1
2	0	1	0	1
3	0	1	1	1
4	1	0	0	1
5	1	0	1	0
6	1	1	0	×
7	1	1	1	×

Truth Table

, 3, 6, 9, 1, 5, ...

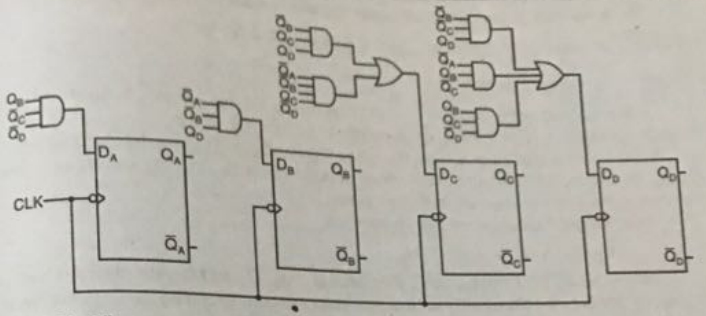
op Inputs	
D_C	D_D
1	1
0	1
0	0
1	0
0	0
0	0
0	1
0	0
0	0
0	1

Q_D $Q_C\overline{Q}_D$
0
0
X
X

$_B Q_D$

$Q_C\overline{Q}_D$
0
1
X
X

$\overline{Q}_C + Q_B Q_C \overline{Q}_D$



Q 61. Why we need shift registers? **(PTU, Dec. 2016)**

Ans. Shift registers are required to shift the data either from left to right or from right to left. The shifting of data is of four basic types :

1. SISO (Serial in serial out)
2. SIPO (Serial in Parallel out)
3. PISO (Parallel in serial out)
4. PIPO (Parallel in Parallel out)

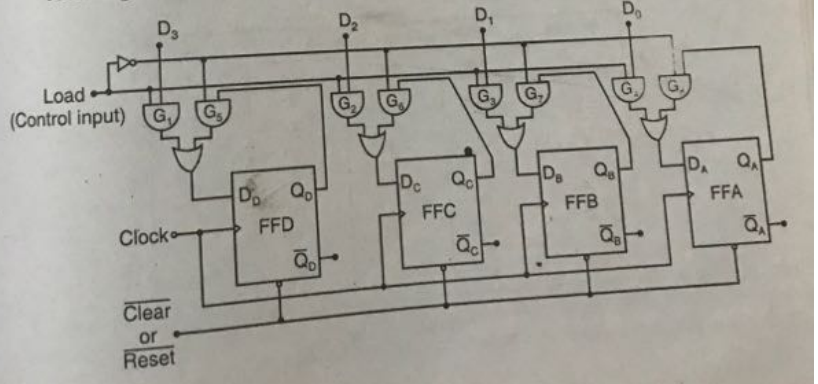
Thus, shift registers are not only used for saving, but for shifting also.

Q 62. Which device can be used to change from serial data to parallel data ? **(PTU, May 2016)**

Ans. Serial in parallel out (SIPO) shift register is used to change from serial data to parallel data.

Q 63. How controlled buffer registers are designed? **(PTU, Dec. 2011)**

Ans. Logic diagram of a controlled buffer register is as shown in fig. for 4-bits



Q 60. Design a synchronous counter using D flip-flop to count 0, 3, 6, 9, 1, 5, ...
Ans.

Present States				Next States				Flip-flop Inputs			
Q_A	Q_B	Q_C	Q_D	Q'_A	Q'_B	Q'_C	Q'_D	D_A	D_B	D_C	D_D
0	0	0	0	0	0	1	1	0	0	1	1
0	0	0	1	0	1	0	1	0	1	0	1
0	0	1	0	0	0	0	0	0	0	0	0
0	0	1	1	0	1	1	0	0	1	1	0
0	1	0	0	0	0	0	0	0	0	0	0
0	1	0	1	0	0	0	0	0	0	0	0
0	1	1	0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	1	0	0	0	1

K-maps are shown below :

For $D_A \rightarrow$

$Q_A Q_B$ \ $Q_C Q_D$	$\bar{Q}_C\bar{Q}_D$	$\bar{Q}_C Q_D$	$Q_C Q_D$	$Q_C\bar{Q}_D$
$\bar{Q}_A\bar{Q}_B$	0	0	0	0
$\bar{Q}_A Q_B$	0	0	0	1
$Q_A Q_B$	X	X	X	X
$Q_A\bar{Q}_B$	0	0	X	X

$\therefore D_A \rightarrow Q_B Q_C \bar{Q}_D$

For $D_B \rightarrow$

$Q_A Q_B$ \ $Q_C Q_D$	$\bar{Q}_C\bar{Q}_D$	$\bar{Q}_C Q_D$	$Q_C Q_D$	$Q_C\bar{Q}_D$
$\bar{Q}_A\bar{Q}_B$	0	1	1	0
$\bar{Q}_A Q_B$	0	0	0	0
$Q_A Q_B$	X	X	X	X
$Q_A\bar{Q}_B$	0	0	X	X

$\therefore D_B \rightarrow \bar{Q}_A \bar{Q}_B Q_D$

For $D_C \rightarrow$

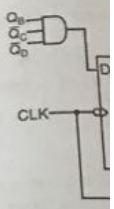
$Q_A Q_B$ \ $Q_C Q_D$	$\bar{Q}_C\bar{Q}_D$	$\bar{Q}_C Q_D$	$Q_C Q_D$	$Q_C\bar{Q}_D$
$\bar{Q}_A\bar{Q}_B$	1	0	1	0
$\bar{Q}_A Q_B$	0	0	0	0
$Q_A Q_B$	X	X	X	X
$Q_A\bar{Q}_B$	0	0	X	X

$\therefore D_C \rightarrow \bar{Q}_B Q_C Q_D + \bar{Q}_A \bar{Q}_B \bar{Q}_C \bar{Q}_D$

For $D_D \rightarrow$

$Q_A Q_B$ \ $Q_C Q_D$	$\bar{Q}_C\bar{Q}_D$	$\bar{Q}_C Q_D$	$Q_C Q_D$	$Q_C\bar{Q}_D$
$\bar{Q}_A\bar{Q}_B$	1	1	0	0
$\bar{Q}_A Q_B$	0	0	0	1
$Q_A Q_B$	X	X	X	X
$Q_A\bar{Q}_B$	0	1	X	X

$\therefore D_D \rightarrow \bar{Q}_B \bar{Q}_C Q_D + \bar{Q}_A \bar{Q}_B \bar{Q}_C + Q_B Q_C \bar{Q}_D$



Q 61. W
Ans. Sh
left. The shifti
1. SISC
2. SIPC
3. PISC
4. PIPC
Thus,
Q 62.

Ans.
parallel data
Q 63.
Ans.

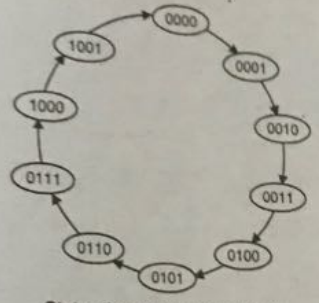
Load
(Control in

Q 71. Which flip flop is preferred for data transfer ? (PTU, Dec. 2016)

Ans. D flip flop is preferred for data transfer. Because if D = 1 then, '1' will be saved in the flip flop and if D = 0 then, '0' will be saved in the flip flop.

Q 72. Design a decade counter using J-K flip-flops. (PTU, Dec. 2012)

Ans. The BCD decade counter counts from 0000 to 1001 as shown in diagram. The invalid states 1010 to 1111 should given next states as 0000 which is done by reset logic connected to clear input of all the flip-flops.



State diagram for valid states

Truth table of BCD counter :

Reset logic output for clear.

Clock	Q_3	Q_2	Q_1	Q_0	$\overline{\text{Clear}}$
0	0	0	0	0	1
1	0	0	0	1	1
2	0	0	1	0	1
3	0	0	1	1	1
4	0	1	0	0	1
5	0	1	0	1	1
6	0	1	1	0	1
7	0	1	1	1	1
8	1	0	0	0	1
9	1	0	0	1	0
10	1	0	1	0	0
11	1	0	1	1	0
12	1	1	0	0	0
13	1	1	0	1	0
14	1	1	1	0	0
15	1	1	1	1	0

of the two stable states unless state is changed by applying external inputs. Thus, it acts as a basic memory element for storage of data in binary form.

Q 67. What is the difference between edge triggering and level triggering? **(PTU, May 2014)**

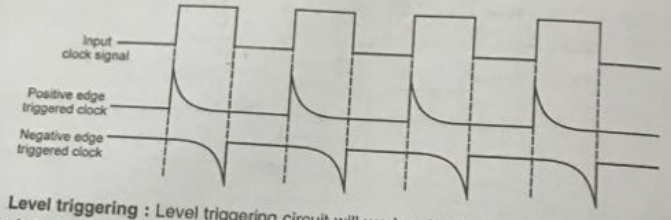
OR

What is edge-triggering? **(PTU, Dec. 2012)**

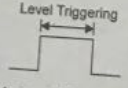
Ans. Triggering is the process of change of state of flip-flop by applying an input-signal. Edge-triggering is obtained by using a differentiator circuit, which make use of R and C passive components. Because RC circuit gives time constant, thus can be used for edge-triggering.

The output from the flip-flop can be obtained by using edge-triggering i.e., either positive edge triggered clock or negative edge triggered clock.

The input clock signal with output spikes or edges is as shown :



Level triggering : Level triggering circuit will work only when Level of clock signal start and before the end.



Q 68. What is the major advantage of D flip-flop over S-R? **(PTU, Dec. 2012)**

Ans. In D flip-flop only two possibilities are there i.e., D = 0 and D = 1. When D is zero, 0 will be stored in the flip-flop with the application of clock pulse. Similarly, when D is one, 1 will be stored in the flip-flop with the application of clock pulse. Where as in S-R flip-flop there are four possibilities and at S = R = 1 the output is indetermined. Which never comes in the D flip-flop.

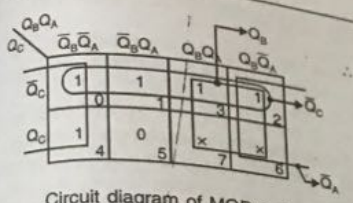
Q 69. What is universal shift register? **(PTU, May 2013)**

Ans. A universal shift register is one which can function in any of the SISO, SIPO, PISO or PIPO modes of operation. To operate the register universally it contains serial input, serial output, parallel inputs, parallel outputs and must be able to serially shift data to the right or to the left, hold the data or to reset. Thus, it has bidirectional property also. It is a 74194 IC.

Q 70. How many flip flops are required for Mod-6 counter?. **(PTU, Dec. 2014 ; May 2013)**

Ans. For MOD-6 the number of flip-flops can be calculated by using the formula $N - 1 \Rightarrow 6 - 1 = 5$.

$(5)_{10} = (101)_2$. It is a three bit data thus three flip-flops are required.

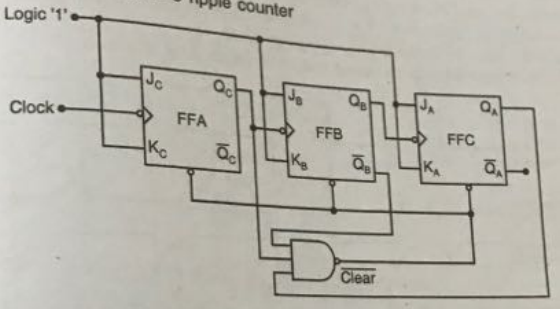


$$\therefore \text{Clear} = \overline{Q}_A + \overline{Q}_B + \overline{Q}_C$$

$$\overline{\text{Clear}} = \overline{\overline{Q}_A + Q_B + \overline{Q}_C} = \overline{\overline{Q}_A} \cdot \overline{Q_B} \cdot \overline{\overline{Q}_C}$$

$$\text{Clear} = \overline{Q_A + \overline{Q}_B + Q_C}$$

Circuit diagram of MOD 5 ripple counter



Q 65. Draw the timing diagram for mod-10 counting. **(PTU, Dec. 2013)**

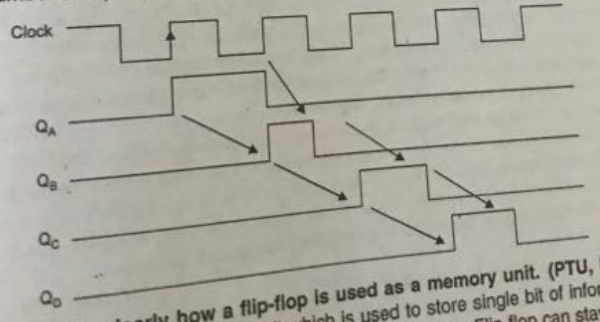
Ans. For mod-10 counter number of flip-flop's required are

$$N \leq 2^n \quad (N = 10)$$

$$10 \leq 2^4$$

$$n = 4$$

So number of flip-flop required are four.



Q 66. Explain clearly how a flip-flop is used as a memory unit. (PTU, Dec. 2012)

Ans. Flip-flop is a sequential circuit which is used to store single bit of information at a time i.e., either '0' or '1' at a time. It has two stable output states. Flip-flop can stay in any one

Q 78. What is the advantage of D flip-flop over S-R ? **(PTU, Dec. 2015)**

Ans. In D flip-flop there is no invalid state, which is the disadvantage of S-R flip-flop. In D flip-flop, if the input is '1' output will be '1' and if the input is '0' output will be '0'. Thus, it is advantage of D flip-flop to save data as per the input provided.

Q 79. What is edge triggering ? How is it different from level clocking ? **(PTU, Dec. 2015)**

Ans. Edge triggering is the type of triggering in which the output will be occurred at a particular edge of clock pulse.

It may be positive edge or negative edge. It is different from level clocking is such a way that the output of level clocking will be occurred during the whole level i.e., either at the high level or at the low level. The complete level will be considered not only a particular edge.

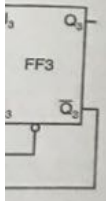
Q 80. Explain the design and working of a 4-bit up-down counter. (PTU, Dec. 2015)

Ans. It can be designed either using J-K flip-flops or T flip-flops. For that excitation ables are required lets design 3-bit synchronous up/down counter using T flip-flops. The citation table for T flip-flop is as shown :

Present State	Next State	Flip Flop Inputs
Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Excitation table of 3-bit up/down counter using T flip-flops.

Mode M Up/Down	Present State			Next State			Flip-Flop inputs		
	Q_C	Q_B	Q_A	Q_{C+1}	Q_{B+1}	Q_{A+1}	T_C	T_B	T_A
0	0	0	0	0	0	1	0	0	1
0	0	0	1	0	1	0	0	1	1
0	0	1	0	0	1	1	0	0	1
0	0	1	1	1	0	0	1	1	1
0	1	0	0	1	0	1	0	0	1
0	1	0	1	1	1	0	0	1	1
1	1	1	1	0	0	0	1	1	1
1	0	0	0	1	1	1	1	1	1
1	0	0	1	0	0	0	0	0	1
1	0	1	0	0	0	1	0	1	1
1	0	1	1	0	1	0	0	0	1
1	1	0	0	0	1	1	1	1	1
1	1	0	1	1	0	0	0	0	1
1	1	1	0	1	0	1	0	1	1
1	1	1	1	1	1	0	0	0	1



2014 ; May 2013)

put depends on ip-flops and the

Dec. 2016, 2014)
d to shift data in
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Triggering and
TU, Dec. 2014)
sed to provide
wo basic types:

Level Triggering is further of two types :
(i) High Level Triggering
(ii) Low Level Triggering.

Difference between Edge Triggering and Level Triggering :

Level Triggering	Edge Triggering
1. It is of two types – High level triggering – Low level triggering	1. It is of two types : – Positive edge triggering – Negative edge triggering
2. The latch or flip-flop circuits which change their outputs only corresponding to active high or low levels are called as level triggered latches or flip-flops.	2. Those flip-flops which change their outputs only corresponding to the positive or negative edge of the clock input are called as edge triggered flip-flops.

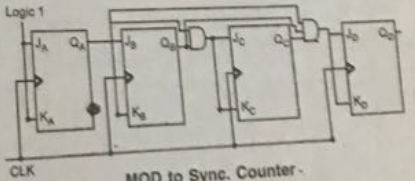
Q 76. Design a MOD-10 synchronous counter using J-K Flip-Flops. Explain its working with the help of timing diagram. **(PTU, Dec. 2014 ; May 2014)**

Ans. MOD-10 means counter will count from 0 to 9.

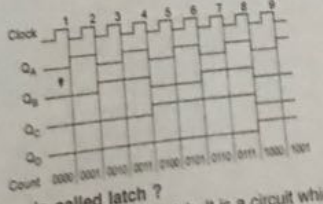
Q_A	Q_B	Q_C	Q_D	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

MOD-10

Donot care XXXX



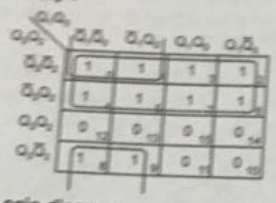
MOD to Sync. Counter



Q 77. Why a flip-flop is called latch ? **(PTU, Dec. 2015)**

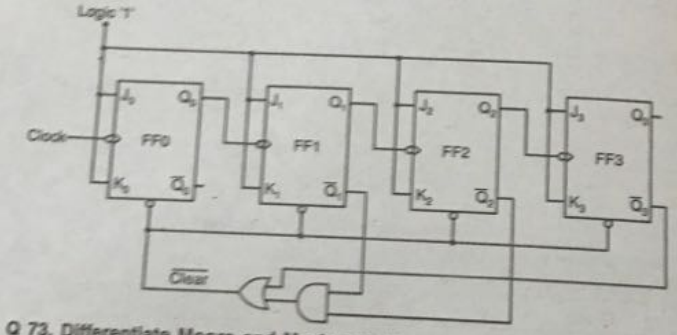
Ans. An unclocked flip-flop is known as latch. It is a circuit which consists of two cross-coupled NAND or NOR gates. Instead of clock signal it has enable signal.

K-map :



$$\therefore \overline{\text{Clear}} = \overline{Q}_3 + \overline{Q}_2\,\overline{Q}_1$$

Logic diagram :



Q 73. Differentiate Moore and Mealy machines. **(PTU, Dec. 2014 ; May 2013)**

Ans.

Moore Machine	Mealy Machine
In Moore machines the output depends only on the present state of the flip-flops.	In Mealy machines the output depends on both the present state of flip-flops and the external inputs.

Q 74. What is Bidirectional shift register ? **(PTU, Dec. 2016, 2014)**

Ans. Bidirectional shift register is a type of shift register which is used to shift data in both the directions i.e., it can shift data from left to right and from right to left.

Q 75. Explain the concept of Triggering ? Also differentiate Edge Triggering and level Triggering.

(PTU, Dec. 2014)

Ans. Triggering is basically required to initiate the circuit. It is used to provide sychronization or timings to the circuit. Triggering is further classified into two basic types: Edge Triggering and Level Triggering.

Edge Triggering is further of two types :

(i) Position Edge Triggering

(ii) Negative Edge Triggering

Level Trigge
(i) High Lev
(ii) Low Lev
Difference

Level Trig
1. It is of two – High lev – Low leve
2. The latch change correspon levels ar latches o

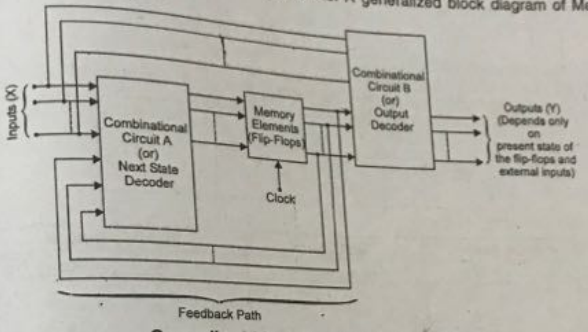
Q 76. De
working with
Ans. MO

Q_A	Q_B	Q_C	Q
0	0	0	
0	0	0	
0	0	1	
0	0	1	
0	1	0	
0	1	0	
0	1	1	
0	1	1	
1	0	0	
1	0	0	
1	0	1	
1	0	1	
1	1	0	
1	1	0	
1	1	1	
1	1	1	

Q 77
Ans.
coupled N

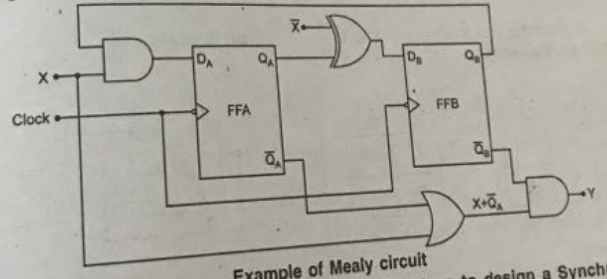
Thus output is derived from present states of the flip-flops or their combination. Here, output Y is combination of flip-flop A and flip flop B outputs. The output appears only when the clock signal is applied.

Mealy Circuit (or Mealy Machine) : When the output of the sequential circuit depends on both the present state of flip-flops and external inputs, then the circuit is called Mealy circuit or the machine is called as Mealy machine. A generalized block diagram of Mealy circuit is as shown in fig.



Generalized block diagram of Mealy Circuit

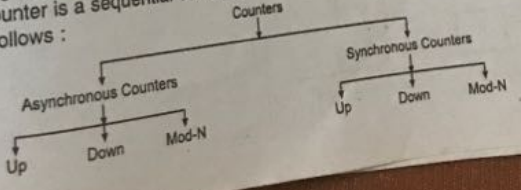
Fig. shows a sequential circuit as an example of Mealy circuit.



Example of Mealy circuit

Q 84. Explain the types of counter. Write the steps to design a Synchronous Counter using JK flip flops. **(PTU, May 2019)**

Ans. Counter is a sequential circuit used to count pulses or clock pulses. Counters are classified as follows :

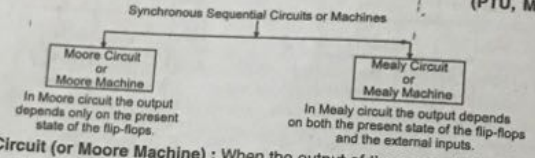


Q 82. What is the purpose of state diagram ? **(PTU, May 2019)**

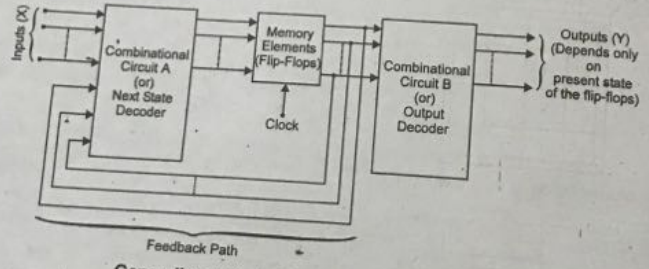
Ans. State diagram is a general model for sequential circuits. In state diagram effect all of previous inputs on the outputs are represented by a state of the circuit. Due to which circuit output at any time depends upon its current input and the current state.

Q 83. What are Mealy and Moore models of sequential circuits ? **(PTU, May 2019)**

Ans.

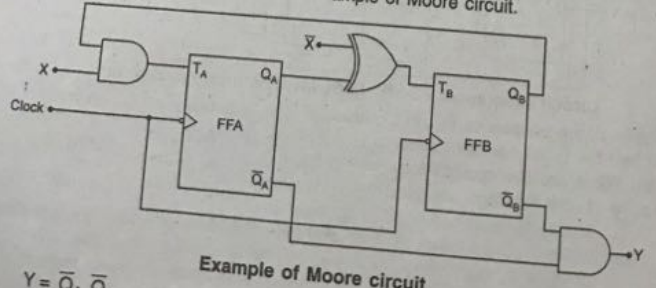


Moore Circuit (or Moore Machine) : When the output of the sequential circuit depends on the present state of flip-flops only, then the circuit is called Moore circuit or the machine is called as Moore machine. A generalized block diagram for a Moore circuit model is shown in fig.



Generalized block diagram of Moore Circuit

Fig. shows a sequential circuit as an example of Moore circuit.



Example of Moore circuit

$Y = \overline{Q}_A \overline{Q}_B$

Thus output is
output Y is combinati
clock signal is applie
Mealy Circuit
on both the present
circuit or the machin
circuit is as shown in

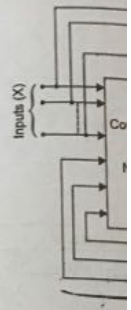
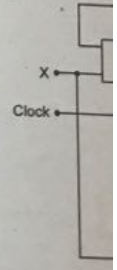
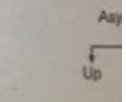


Fig. shows a



Q 84. Expla
Counter using JK
Ans. Counte
classified as follow



(PTU, Dec. 2015)

ntage of S-R flip-flop. In
ut will be '0'. Thus, it is

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(PTU, Dec. 2015)

t will be occurred at a

clocking is such a way
i.e., either at the high
a particular edge.

ter. (PTU, Dec. 2015)

s. For that excitation
sing T flip-flops. The

nputs

Flip-Flop inputs	
T_B	T_A
0	1
1	1
0	1
1	1
0	1
1	1
1	1
1	1
0	1
1	1
0	1
1	1
0	1
1	1
0	1

K-maps are as follows :

For $T_C \rightarrow$

MQ_C \ Q_BQ_A	$\bar{Q}_B\bar{Q}_A$	$\bar{Q}_BQ_A$	Q_BQ_A	$Q_B\bar{Q}_A$
$M\bar{Q}_C$	0	0	1	0
$\bar{M}Q_C$	0	0	1	0
MQ_C	1	0	0	0
$M\bar{Q}_C$	1	0	0	0

$\therefore T_C = \bar{M}Q_BQ_A + M\bar{Q}_B\bar{Q}_A$

For $T_B \rightarrow$

MQ_C \ Q_BQ_A	$\bar{Q}_B\bar{Q}_A$	$\bar{Q}_BQ_A$	Q_BQ_A	$Q_B\bar{Q}_A$
$M\bar{Q}_C$	0	1	1	0
$\bar{M}Q_C$	0	1	1	0
MQ_C	1	0	0	1
$M\bar{Q}_C$	1	0	0	1

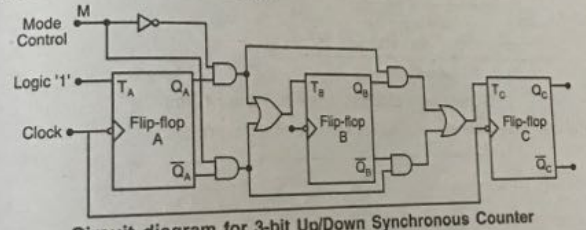
$\therefore T_B = \bar{M}Q_A + M\bar{Q}_A = M \oplus Q_A$

For $T_A \rightarrow$

MQ_C \ Q_BQ_A				
	1	1	1	1
	1	1	1	1
	1	1	1	1
	1	1	1	1

$\therefore T_A = 1$

Implementation is as shown in fig.



Circuit diagram for 3-bit Up/Down Synchronous Counter

For M = 0, the counter counts in Up mode.
and for M = 1, the counter counts in Down mode.

Q 81. What are the applications of flip-flops ? (PTU, Dec. 2017)

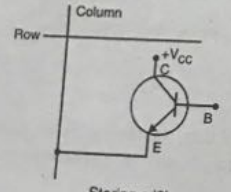
Ans.
- 1. J-K flip-flops are used in shift registers.
  2. J-K flip-flops are used in counters.
- D flip-flops are delay flip flops and are extensively used for temporary storage of data in registers. Hence, registers make use of D flip-flops.
- T flip-flops are toggle flip-flops and are used in counters. Hence, counter designing make use of T flip-flops.

- In masked ROM the data is stored permanently through photomasking during fabrication i.e. prorammning is done through masking and metalization process.
- PROM is the programmable read only memory. It is programmed using PROM-programmer and once the data is programmed (i.e. written) cannot be rewrite or changed again.
- EPROM is the erasable programmable read only memory. The user can erase and programme this memory again and again. The EPROM is erased by exposing the chip from inside via window at the top to ultra violet light.
- EEPROM is the electrically erasable programmable read only memory. Its function is similar to EPROM but instead UV light the data can be erased using electrical signals.
- PLAs are programmable logic arrays in which AND-OR gate arrays are used and programmed for specific logic functions.
- PLDs are the programmable logic devices. There are of three types :
  (a) PAL
  (b) PLA
  (c) PGA or FPGA.
- PAL are the programmable arary logic in which AND gate arrays are programmable and OR gate arrays are fixed.
- FPGA is the field programmable gate array. It consists of logic blocks i.e. an array of circuit elements.

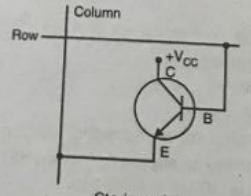
QUESTION-ANSWERS

Q 1. Explain the Bipolar RAM Cell.

Ans. Bipolar transistor is used in bipolar ROM cell. It is as shown in figure.



Storing a '0'



Storing a '1'

When base of transistor is not connected with a row no current flows to the base and thus, it represents a storage of logic '0'. On the other hand, when base is connected the current starts flowing to the base of transistor and it represents a storage of logic '1'.

Q 2. Why do we use PGAs? **(PTU, May 2012)**

Ans. PGA's are programmable gate arrays and are consists of logic blocks called as an array of circuit elements. PGA's are used to implement large logic circuits because of their high logic densities i.e. 10×10^3 to few 100×10^3 equivalent gates on a single chip.

Q 3. Design the O

Ans. These gives t

Outputs of AND arrays

OR arrays gives

Here 'X' are the f
fuses or blown off fus

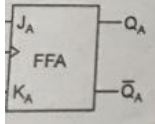
Q 4. Draw the

Ans.

count.)

Inputs $J_B K_B$

puts J_B	K_B
1	x
x	1
1	x
x	1



Chapter 6

Memory Devices

Contents

Classification of memories, RAM organization, Write operation, Read operation, Memory cycle. ROM organization, PROM, EPROM, EEPROM, Programmable logic array, Programmable array logic, complex Programmable logic devices (CPLDS), Field Programmable Gate Array (FPGA).

POINTS TO REMEMBER

- Memory is used for storing binary words.
- Memory size is specified by the number of words i.e. 'M' and the number of bits per word i.e. 'N', such as : M × N.
- Reading is the process by which the data can be retrieved from memory.
- Writing is the process by which the data can be stored in the memory.
- Semiconductor memories make use of bipolar and MOS.
- Types of memories :
  (a) RAM
  (b) ROM
- RAM is the random access memory or read/write memory. One can read and write in RAM.
- ROM is the read only memory. One can only read from ROM nothing can be written in it.
- RAM is of two types :
  (a) SRAM
  (b) DRAM
- SRAM is also known as static RAM. In SRAM data will remain stored permanently as long as power is supplied, they need not required rewriting periodically the data. The basic cell is SRAM is a flip-flop.
- DRAM is also known as dynamic RAM. In DRAM rewriting periodically the data into memory is required. The basic cell in DRAM is a capacitor.
- ROM is of four types :
  (a) Masked ROM
  (b) PROM
  (c) EPROM
  (d) EEPROM

Steps to design synchronous counter using J-K flipflop.

(1) Firstly design a table as shown : (Lets take 2 bit synchronous count.)

Present States		Next States		Flip-flop Inputs	
Q_A	Q_B	Q_{A+1}	Q_{B+1}	J_AK_A	J_BK_B
0	0	0	1		
0	1	1	0		
1	0	1	1		
1	1	0	0		

(2) From excitation table of J-K complete the above table

Present State	Next State	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

(3) After putting we get :

Present States		Next States		Flip-flop Inputs			
Q_A	Q_B	Q_{A+1}	Q_{B+1}	J_A	K_A	J_B	K_B
0	0	0	1	0	x	1	x
0	1	1	0	1	x	x	1
1	0	1	1	x	0	1	x
1	1	0	0	x	1	x	1

Put the flip flop inputs in K-map to implement the circuit

For J_A :

Q_A \ $Q_B\bar{Q}_B$	Q_B
$\bar{Q}_A$	0 (1)
Q_A	X (X)

$\therefore J_A = Q_B$

For K_A :

Q_A \ $Q_B\bar{Q}_B$	Q_B
$\bar{Q}_A$	X (X)
Q_A	0 (1)

$\therefore K_A = Q_B$

Similarly,

For J_B :

Q_A \ Q_B	
1	X
1	X

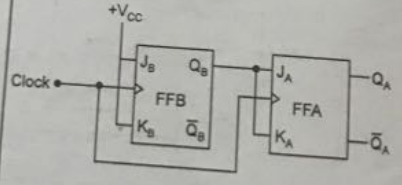
$\therefore J_B = 1$

For K_B :

Q_A \ Q_B	
X	1
X	1

$\therefore K_B = 1$

Circuit is as shown



❑❑❑

Chapter 6

Contents

Classification of m
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array logic, compl
(FPGA).

- Memory is us
- Memory size
  i.e. 'N', such
- Reading is th
- Writing is the
- Semiconduct
- Types of me
  (a) RAM
  (b) ROM
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- RAM is of tw
  (a) SRAM
  (b) DRAM
- SRAM is al
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- DRAM is a
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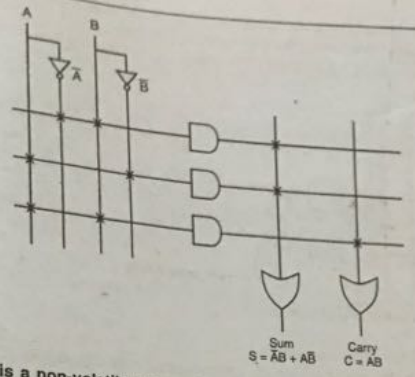
- ROM is of
  (a) Masked
  (b) PROM
  (c) EPROM
  (d) EEPRO



Q 7. What is a non-volatile memory? **(PTU, May 2014, 2009)**

Ans. Non-volatile memory : The memory in which the data stored or information present once does not change even after the power is switched off is called as non-volatile memory.

ROM i.e. Read only memory is the example of non-volatile memory. Because such memories hold the data or information even if power is switched off.

Q 8. What are the advantages of static RAM over Dynamic RAM? **(PTU, May 2015, 2014, 2007)**

Ans. Advantages of static RAM over Dynamic RAM :

1. Access time of SRAM is less and thus these memories are faster memories.
2. As SRAM is consists of flip-flops thus, refreshing is not required.
3. Less number of memory cells are required in SRAM for unit area.

Q 9. What is EEPROM? **(PTU, May 2017, 2014 ; Dec. 2006)**

Ans. EEPROM : Electrically Erasable PROM or Electrically Erasable Programmable Read Only Memory. This memory stores a bit by charging the floating gate of an FET. Thus, the memory is similar to EPROM except that the information can be altered by using electrical signals at the register level rather than erasing all the information i.e. it can be erased information byte to byte.

Q 10. What is PAL? **(PTU, May 2006)**

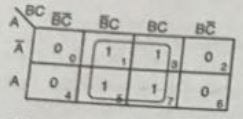
Ans. PAL : PAL is known as programmable array logic. It is a programmed logic device with OR arrays fixed and AND arrays programmable. Because only AND gates are programmable, the PAL is easier to program, but it is not as flexible as the PLA (programmable logic array).

Q 5. Implement the boolean function using PAL.

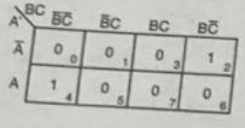
$Y_1 = \Sigma m\ (1, 3, 5, 7)$

$Y_2 = \Sigma m\ (2, 4).$

Ans. Let the input variables are A, B and C. The K-map minimization is as shown :

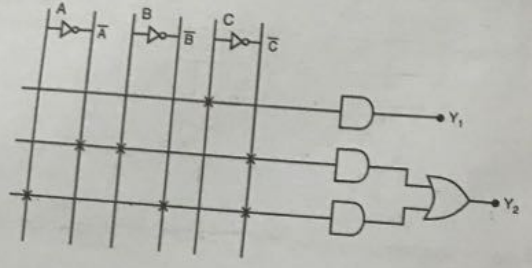


$\therefore Y_1 = C$



$\therefore Y_2 = \overline{A}B\overline{C} + A\overline{B}\overline{C}$

Implementation using PAL :



Q 6. Design half adder circuit using PLA.

Ans. Truth table of Half Adder circuit is :

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

$\therefore$ Sum = $S = \overline{A}B + A\overline{B}$

and Carry = $C = AB$.

Q 7. What i

Ans. Non-v

present once does

memory.

ROM i.e. Re

memories hold the

Q 8. What a

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1. Access tir
2. As SRAM
3. Less num

Q 9. What is

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Read Only Memor

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Q 10. What

Ans. PAL :

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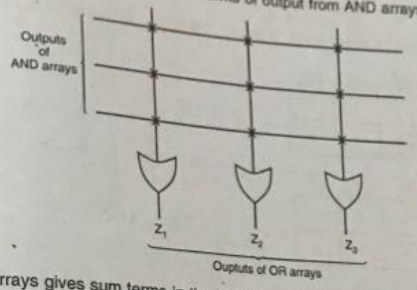
n figure.

s to the base and
is connected the
of logic '1'.

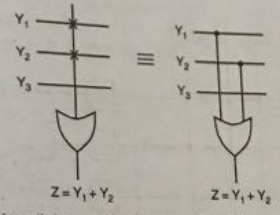
(PTU, May 2012)
locks called as an
because of their
single chip.

Q 3. Design the OR Matrix or OR array.

Ans. These gives the logical sum terms of output from AND arrays as shown in fig.



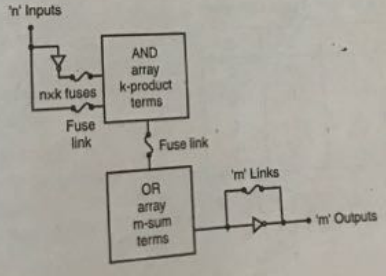
OR arrays gives sum terms in the logical form. Such as :



Here 'X' are the fuse links used in diagrams. The interconnections without 'X' are unpluged fuses or blown off fuse links.

Q 4. Draw the block diagram of PLA logic device.

Ans.



Q 16. Explain the different types of ROMs. Discuss their advantages and disadvantages. **(PTU, May 2014, 2011)**

OR

What is ROM? Explain all types of ROMs. **(PTU, Dec. 2016, 2006, 2005)**

Ans. ROM : In ROM, read and write operation cannot be performed with equal ease always read operation is easier than write operation. It is used to store information which is (i) Permanent group includes ; masked ROM and PROM (ii) Semi permanent group include ; EPROM and EE-PROM. Five types of ROM-masked ROM, PROM, EPROM, EE-PROM and flash memory are described in the following paragraphs.

Masked ROM : Programming is done through masking and metallization process. Manufactures provides programmed ROM, user cannot write into this memory.

PROM : Programmable Read Only Memory user can program (write) the PROM through special PROM programmer. It can be written (programmed) once only, user cannot rewrite this memory.

EPROM : Erasable Programmable ROM. This memory stores a bit by charging the floating gate of an FET. The chip can be reused may times i.e., user can write this memory many time.

Erasing is done using UV light through a window over the memory chip called quartz window. Erasing process cannot be done byte by byte or block by block, entire information will be erased at once, after exposing the ROM in U.V. light. Therefore, erasing process is slower and time consuming it takes 15 to 20 minutes.

EEPROM : Electrically Erasable PROM. This memory is functionally similar to EPROM, except that information can be altered by using electrical signals at the register level rather than erasing the information i.e., it can be erased information byte to byte.

Q 17. Explain about associative memory. **(PTU, May 2006)**

Ans. Associative Memory : CAM is the associative memory. CAM (i.e. Content Addressable Memories) is a type of memory in which any memory location can be accessed by looking for the actual data. To find the appropriate location, the input data, called as key is compared with all the stored data words. Whenever a match occurs, an output signal is produced. This operation is referred as association and thus the memory is called as associative memory.

After selecting the locations by matching the contents with the key, the read or write operation can be performed. CAM can perform :

1. Write
2. Read and
3. Associate.

Q 18. Describe the advantage of using PLA over ROM for realizing some Boolean functions. **(PTU, May 2005)**

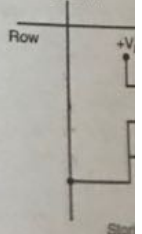
Ans. Advantages of using PLA over ROM :

1. It is easy to design the ROM using PLA. The design becomes very easy.
2. Using PLA the cost reduces.
3. The design can be modify or change very quickly. It takes less time as compared to SSI/MSI chips for modification.
4. The switching speed becomes high.

5. It gives higher dens
6. Larger flexibility car
7. Less space is requi

Q 19. Implement the
F = A'BC + ABC' + A
Ans. F =
Implementation using

Q 20. Explain how
Ans. EPROM mem
by using PROM program
charging the floating gate.
It is erased and rep
UV) through a small wind
MOS ROM cell is a



Stor

ng PAL. It is as shown :

$\bar{B}C$	$B\bar{C}$	
1	1	0
0	0	1

$\bar{A}C + A\bar{C}$

(PTU, May 2006)

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nory

(PTU, Dec. 2005)

AND array only as a

are programmable.

(PTU, Dec. 2004)

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PAL.

Q 14. What do you mean by PLD's? (PTU, May 2005)

Ans. PLDs : Programmable logic devices are the special type of IC's used by the user and are programmed before use. Different type of logic functions can be implemented using a single programmed IC chip of PLD's. PLD's can be reprogrammed because these are baesd on re-writable memory technologies. Fuse links are used to programmed the PLD by the user according to the type of PLD to be manufactured.

Q 15. Describe with diagram internal architecture of PLA. (PTU, May 2009)

Ans. PLA is Programmable Logic Array. It is used where the number of don't care conditions are excessive. In PLA's both AND and OR arrays are programmable. The AND and OR gates are fixed for any PLA chip. It depends on the number of inputs and outputs of PLA.

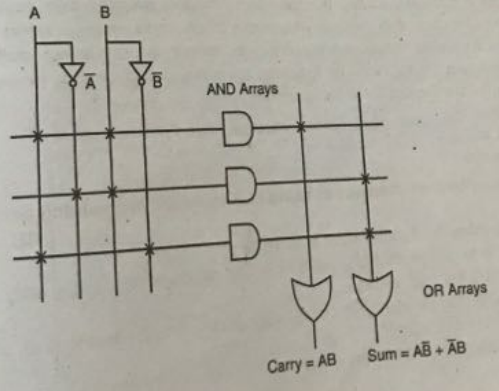
Let us take an example of Half Adder to illustrate the diagram internal architecture of PLA :

Truth Table of Half Adder :

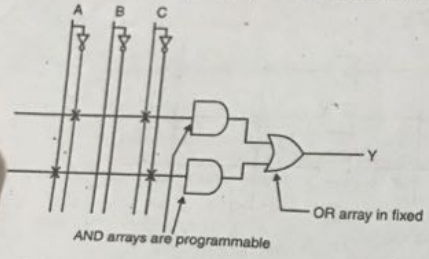
Inputs		Outputs	
A	B	Carry	Sum
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Thus, carry = A . B and sum = $\bar{A}B + A\bar{B}$

Implementation of Half Adder using PLA is as shown :



For example : We have a boolean function given by
$Y(A, B, C,) = \Sigma m\ (1, 3, 4, 6)$ and we have to implement it by using PAL. It is as shown :

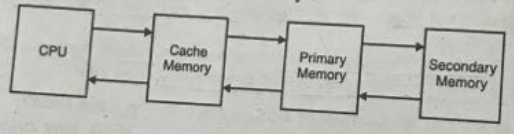


A \ BC	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	0	1	1	0
A	1	0	0	1

$\therefore \quad Y = \bar{A}C + A\bar{C}$

Q 11. What is cache memory? **(PTU, May 2006)**

Ans. Cache memory is a type of semiconductor memory. It forced its entry as fast memory device. It works as an interface between the CPU and the primary memory. Following block diagram shows the position of cache memory :



Q 12. Explain the role of PAL and PLA in digital design. **(PTU, Dec. 2005)**

Ans. PAL : It is called programmable array logic . It make use of AND array only as a programmable but OR array is fixed.

PLA : It is called programmable logic array. Its AND or OR array both are programmable.

Both PAL and PLA are used for memory purposes.

Q 13. What is the difference between PAL and PLA? **(PTU, Dec. 2004)**

Ans.

PLA	PAL
1. In case of PLA i.e. programable logic array both AND and OR arrays are programmable.	1. In case of PAL i.e. programmable array logic OR arrays are fixed and and AND arrays are programmable.
2. It is costlier as compared to PAL.	2. It is cheaper.
3. It is complex than PAL.	3. It is simple.
It can't easily be programmed.	4. It is easy to program a PAL.

Q 14. What d

Ans. PLDs : P

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the user according t

Q 15. Describ

Ans. PLA is
conditions are exce
and OR gates are fi
PLA.

Let us take a
PLA :

Truth Table of

Thus, carry =

Implementati

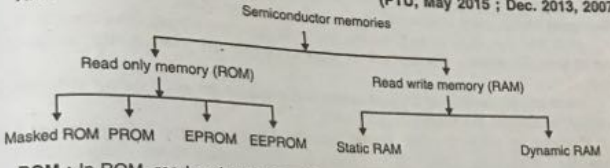
A

$$\frac{16K}{2K} = 8.$$

Thus, 8 PROM chips are required.
Each chip is having address lines which can be calculated by calculating the total
i.e. $16K = 16 \times 1024 = 16384$
Also, $16384 = 2^{14}$.
Therefore, 14 address lines are required.

Q 23. Name and discuss the various types of semiconductor memories.

Ans. **(PTU, May 2015 ; Dec. 2013, 2007)**



ROM : In ROM, read and write operation cannot be performed with equal ease always read operation is easier than write operation. It is used to store information which is (i) Permanent group includes ; masked ROM and PROM (ii) Semi permanent group include ; EPROM and EE-PROM. Five types of ROM-masked ROM, PROM, EPROM, EE-PROM and flash memory are described in the following paragraphs.

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EEPROM : Electrically Erasable PROM. This memory is functionally similar to EPROM, except that information can be altered by using electrical signals at the register level rather than erasing the information i.e., it can be erased information byte to byte.

RAM :

1. Static RAM : In SRAM the stored data will remain permanently stored as long as power supplied, there is no need to write the data periodically into memory. SRAM is basic

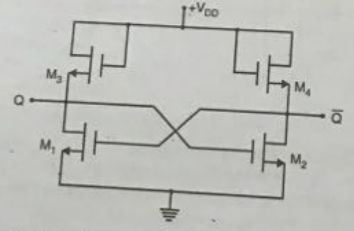
It works in the similar manner as bipolar ROM cell. If the gate is connected with row line it stores '1' and if the connection is absent, it stores logic '0'.

Q 21. Differentiate between static MOS and Dynamic MOS RAM. Draw the circuit of a static MOS RAM cell and explain its working. (PTU, Dec. 2014 ; May 2013, 2008)

Ans.

Static MOS RAM	Dynamic MOS RAM
1. SMOS RAM doent use capacitor in the circuit.	1. DMOS RAM make use of capacitor in the circuit.
2. SMOS RAM make use of more number of components per cell.	2. It uses less as compared to SMOS RAM.
3. Refreshing is not required in SMOS RAM.	3. Refreshing is required as capacitor is used in DMOS RAM.
4. Cost is more.	4. Cost is less.
5. Consumes more power than DMOS RAM.	5. Low power consumption is the advantage over SMOS RAM.

Following figure shows the circuit of a static MOS RAM cell.



Cross-coupled latch is formed by using M_1 and M_2 MOSFET's (Metal oxide semiconductor field effect transistor). M_1 and M_2 works as switches. M_3 and M_4 replaces the resistors R_1 and R_2 of a bipolar SRAM cell and are used to serve as active loads. At a time one MOSFET i.e., either M_1 or M_2 will be ON. When the OFF MOSFET is made ON by providing some external means, it forces the ON MOSFET to OFF state. This clears that it has two stable states for the storage of data or information.

Q 22. The capacity of 2K x 16 PROM is to be expanded to 16K x 16. Find the number of PROM chips required and the number of address lines in the expanded memory. (PTU, May 2008)

Ans. The capacity of 2K x 16 PROM is to be expanded to 16K x 16.

Thus, the capacity of given chip is 2K and a capacity of 16K is required. Hence, the number of chips required are given by :

Thus, 8 PRC
Each chip is
i.e.
Also,
Therefore, 1

Q 23. Name

Ans.

Read

Masked ROM P

ROM : In RO
read operation is
Permanent group
EPROM and EE-P
flash memory are

Masked RO
Manufactures prov

PROM : Prog
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EPROM : E
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Erasing is do
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EEPROM : E
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than erasing the in

RAM :

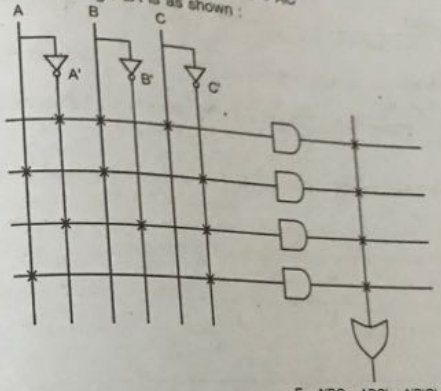
1. Static RA
power supplied, th

5. It gives higher density using PLA.
6. Larger flexibility can be achieved using PLA over ROM.
7. Less space is required for designing the circuits.

Q 19. Implement the function
F = A'BC + ABC' + A'B'C' + AC' using PLA. **(PTU, Dec. 2009 ; May 2009)**

Ans. F = A'BC + ABC' + A'B'C' + AC'

Implementation using PLA is as shown :

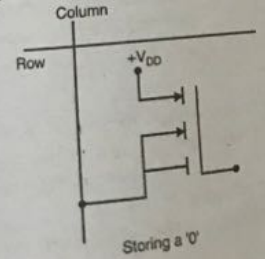


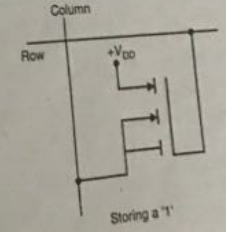
Q 20. Explain how EPROM memory cell works. **(PTU, May 2017 ; Dec. 2008)**

Ans. EPROM memory cell : It is the erasable type of ROM. The programming is done by using PROM programmes. FET is used in the memory cell for storage. It stores a bit by charging the floating gate. Thus, the chip can be used many times.

It is erased and reprogrammed by exposing the chip from inside to ultra violet light (i.e. UV) through a small window on the top of chip.

MOS ROM cell is as shown which is used for EPROM memory cel.





The address is specified in the binary form. The number of distinct address possible with 'n' input variable is 2^n.

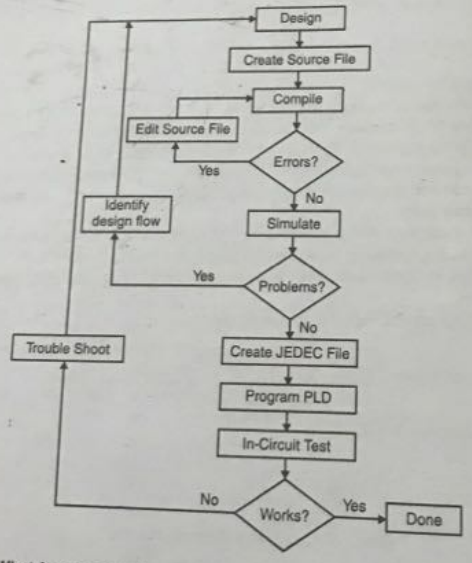
Each bit combination that comes out of the output line is called word, therefore number of bits per word is equal to number of output lines.

In computer system we define 1024 as 1K ; therefore 1K-byte memory chip has 1024 registers with 8 bits each. Similarly, a group of 256 registers is defined as one page and each register is viewed as a line to write on.

The total capacity of memory having R address lines and N data lines is defined as $2^R \times N$.

Q 26. Give the flow chart of PLD design, programming and test process.
(PTU, May 2005 ; Dec. 2005)

Ans. PLD development cycle flow chart is as shown :



Q 27. What is the advantages of using Gate Array in digital design?
(PTU, Dec. 2004)

Ans. Advantages of using Gate Array in digital design :

1. The effective size can
2. Number of functions c
3. Gate arrays have ver

equivalent gates.

4. The gate arrays dosn

for implementing the given bo

5. More number of arr

available in Gate arrays for d

Q 28. A computer emp
computer system needs 2K
each with four registers. A
order bits of the address bu
registers. How many RAM

Ans. RAM chips empl
ROM chips employed
Requirement of RAM
Reqiurement of ROM
Total number of RAM

=

∴ Number of RAM ch
Total numbers of RO

∴ Number of ROM c

Q 29. What are th
EEPROMS.

Ans. Advantages o

1. Flash memory is s

continuously.

2. The erasing and
3. Flash memories
4. Flash memory is hi
5. Flash memory is u

are used for reading purp

Q 30. What is a vo

Ans. The memory i

is switched off is called a

of volatile memory. Beca

off.

aster as compare to

tly stored unless the
y cell. It uses 4 MOS
t is less and circuit is

. Also show how a
(PTU, May 2007)
ammable AND matrix
any OR gates. PAL

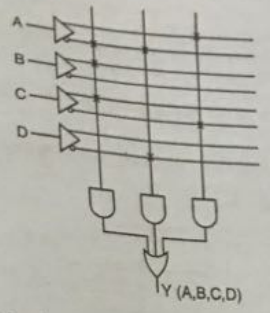
R gates can share a
t must be generated

utput OR gate, it is

ND gates and 2 fixed

$C + \overline{A}\,\overline{D} + A\overline{C}$

Following fig. shows the PAL having 4 inputs (A, B, C and D), 3 programmable AND gates and 1 fixed OR gate.

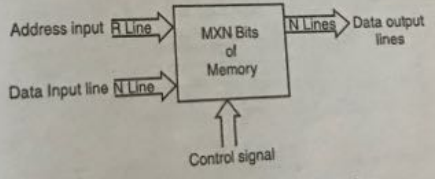


Q 25. Explain about memory organisation. **(PTU, Dec. 2017 ; May 2006)**

Ans. Memory Organization : The basic element of a semiconductor memory is a flip-flop. The information is stored in a binary form. There are a number of locations in a memory chip, each location being meant for one word of digital information. Memory chips are available in various word sizes and the size of a memory chip is generally specified in terms of the total number of bits it can store.

The size of a memory chip is specified by two numbers M and N as M × N bits. The number M specifies the number of locations available in the memory and N is the number of bits at each location. In other words, this means that M words of N bits each can be stored in the memory.

The block diagram of a memory device as shown in fig.



Block diagram of a memory device

Each of the M locations of the memory is defined by unique address and therefore, for accessing any one of the M locations, R inputs are required, where $M = 2^R$. This set of lines is referred to as address line. The number of inputs required to store the data into or read the data from any memory location is N.

memory cell consists of flip-flops. One SRAM uses 6 transistors. It is faster as compare to DRAM and also more expensive and high durability.

2. Dynamic RAM : In DRAM the data will not remain permanently stored unless the data rewritten into memory periodically. It consists of capacitor as memory cell. It uses 4 MOS transistors. Its power consumption in low as compared to SRAM. Its cost is less and circuit is not complex as compared to SRAM.

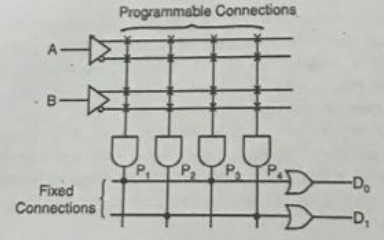
Q 24. Discuss the programmable array logic device in detail. Also show how a combinational circuit is implemented using PAL. **(PTU, May 2007)**

Ans. Programmable Array Logic (PAL) : This device has a programmable AND matrix and a fixed OR plane. All the AND gates outputs are not connected to any OR gates. PAL offers good flexibility and cost is less and speed is fast than PLAs.

As in PAL the inputs to the OR gates are fixed, therefore, no two OR gates can share a product term. So when a product term is required by two OR gates, it must be generated twice.

Since limited number of product terms are available for each output OR gate, it is necessary to simplify the function.

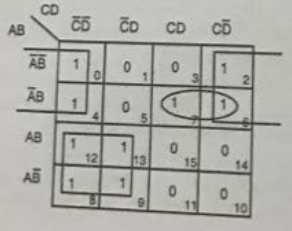
Following fig. shows the PAL having 2-inputs, 4 programmable AND gates and 2 fixed OR gates.



For example : Implement the following function using PAL.

$Y(A, B, C, D) = \Sigma m (0,2, 4, 6, 7, 8, 9, 12, 13)$.

Solution. First put the min terms in a K-map for minimization



$\therefore Y(A, B, C, D) = \overline{A}BC + \overline{A}\overline{D} + A\overline{C}$

and are programmed before use. Different type of logic functions can be implemented using a single programmed IC chip of PLD's. PLD's can be reprogrammed because these are baesd on re-writable memory technologies. Fuse links are used to programmed the PLD by the user according to the type of PLD to be manufactured.

PLA is Programmable Logic Array. It is used where the number of don't care conditions are excessive. In PLA's both AND and OR arrays are programmable. The AND and OR gates are fixed for any PLA chip. It depends on the number of inputs and outputs of PLA.

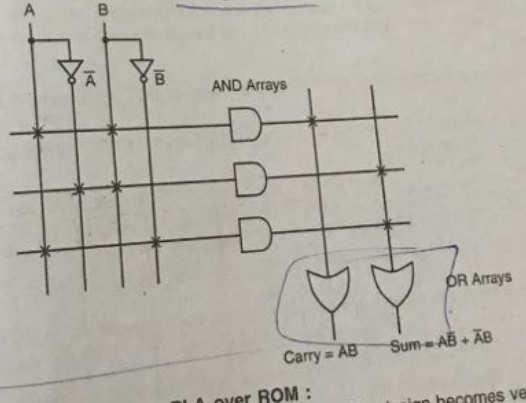
Let us take an example of Half Adder to illustrate the diagram internal architecture of PLA :

Truth Table of Half Adder :

Inputs		Outputs	
A	B	Carry	Sum
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Thus, carry = A . B and sum = $\overline{A}B + A\overline{B}$

Implementation of Half Adder using PLA is as shown :



Advantages of using PLA over ROM :

1. It is easy to design the ROM using PLA. The design becomes very easy.
2. Using PLA the cost reduces.
3. The design can be modify or change very quickly. It takes less time as compared to SSI/MSI chips for modification.
4. The switching speed becomes high.
5. It gives higher density using PLA.

Q 31. Write pros and cons of SRAM and DRAM cell. **(PTU, May 2010)**

Ans. Pros and Cons means advantages and disadvantages.

Advantages of SRAM :

1. Refreshing is not required.
2. Less access time is required and thus, these are faster memories.

Dis-advantages of SRAM :

1. Number of components per cell required are more.
2. Cost is more.

Advantages of DRAM :

1. Cost is less.
2. Number of components required per cell are less i.e. only two.

Dis-advantages of DRAM :

1. Refreshing is required.
2. Access time required is more and thus are slower memories.

Q 32. Write the full form of EEPROM, PAL, PGA and PLD. **(PTU, Dec. 2010)**

Ans. EEPROM : Electrically Erasable Programmable Read Only Memory

PAL : Programmable Array Logic

PGA : Programmable Gate Array

PLD : Programmable Logic Devices.

Q 33. How ROM is different from RAM? **(PTU, May 2011)**

Ans.

RAM	ROM
(i) RAM is random access memory.	(i) ROM is read only memory.
(ii) In RAM data can be read/write at any time during the operation of system.	(ii) In ROM data can be read only. One can't write in ROM after the chip is ready to use.
(iii) RAM is volatile memory.	(iii) ROM is non-volatile memory.
(iv) RAM types are S-RAM and D-RAM.	(iv) ROM types are PROM, EPROM, EEPROM etc.

Q 34. Explain the difference between EPROM and EEPROM. **(PTU, Dec. 2010)**

Ans.

EPROM	EEPROM
(a) It is called as erasable programmable read only memory.	(a) It is called as electrically erasable programmable read only memory.
(b) EPROM chip uses UV light for erasing the data contents.	(b) EEPROM uses electrical signals for erasing the data contents.
(c) The erasing process in EPROM takes 15 to 20 minutes.	(c) The erasing process in EEPROM is done byte to byte. Thus faster.

Q 35. What are programmable logic devices. What are their advantages? Explain in detail the architecture of a programmable logic device. **(PTU, May 2018, 2010)**

Ans. PLDs : Programmable logic devices are the special type of IC's used by the user

distinct address possible

word, therefore number

memory chip has 1024
d as one page and each

data lines is defined as

d test process.
May 2005 ; Dec. 2005)

e

design?
(PTU, Dec. 2004)

1. The effective size can be increased by using gate arrays.
2. Number of functions can be increase by using gate arrays.
3. Gate arrays have very high logic densities, i.e. from 10^4 to few hundred thousand equivalent gates.
4. The gate arrays dosn't contain the AND or OR matrices. It make use of logic blocks for implementing the given boolean function.
5. More number of architectures, packagings and programming technologies are available in Gate arrays for digital design.

Q 28. A computer employs RAM chips of 256 × 8 and ROM chips of 1024 × 8. The computer system needs 2K bytes of RAM, 4K bytes of ROM and four interface units, each with four registers. A memory-mapped I/O configuration is used. The two highest order bits of the address bus are assigned 00 for RAM, 01 for ROM and 10 for interface registers. How many RAM and ROM chips are needed? (PTU, May 2005)

Ans. RAM chips employed by computer having memory = 256 × 8
ROM chips employed by computer having memory = 1024 × 8
Requirement of RAM = 2K bytes = 1024 × 2
Reqiurement of ROM = 4K bytes = 1024 × 2 × 2
Total number of RAM chips needed are given by :

$$= \frac{1024 \times 2}{256} = 8$$

∴ Number of RAM chips needed are : 8
Total numbers of ROM chips needed are given by :

$$= \frac{1024 \times 2 \times 2}{256} = 4$$

∴ Number of ROM chips needed are : 4.

Q 29. What are the advantages of using flash memory over EPROM and EEPROMS. (PTU, Dec. 2004)

Ans. Advantages of using flash memory over EPROMs and EEPROMs :

1. Flash memory is special type of RAM and is a non-volatile memory which is powered continuously.
2. The erasing and programming of flash memory takes place block by block.
3. Flash memories are faster than EEPROMs.
4. Flash memory is high speed, low operating voltages, durable and low power consumption.
5. Flash memory is used for reading and writing operations but EPROMs and EEPROMs are used for reading purposes only.

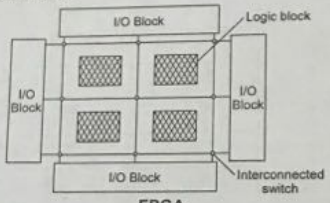
Q 30. What is a volatile memory? (PTU, May 2016, 2015 ; Dec. 2009)

Ans. The memory in which the data stored or information present changes when power is switched off is called as volatile memory. RAM i.e. random access memory is the example of volatile memory. Because such memories lost the data or information if power is switched off.

Q 40. Write a short note on Field Programmable Gate Array.
(PTU, May 2018, 2017, 2014)

Ans. Field programmable gate array consist of logic blocks i.e. an array of circuit element. These logic blocks are simply the gate array, but programming is done by the customer and not by the manufacturer.

Static RAM (SRAM) or antifuse are used as switches for interconnection of blocks. FPGA are used to implement large logic circuit because of their very high logic density. Thus it is advantageous to use FPGA for custom made integrated circuits due to which large hardware system are eliminated.



FPGA

FPGA is a e.g. of sequential programable device i.e. SPD.

Q 41. How many 256×8 memory chips are required to obtain a 2048×8 memory ?
(PTU, May 2015)

Ans. The capacity of 256×8 memory chips is to be expanded to 2048×8 memory chips. Thus, the capacity of given chip is 256 and a capacity of 2048 is required. Hence, the number of chips required are given by : $\frac{2048}{256} = 8$.

Thus, 8 memory chips are required.

Q 42. What is the difference between PROM and EPROM ? **(PTU, May 2016)**

Ans.

PROM	EPROM
(i) It can be programmed to record data using a PROM programmer once only and cannot be changed or rewrite again	(i) It can be erased and programme the memory again and again.
(ii) Not used UV light for erasing.	(ii) Used UV light for erasing the memory contents.

Q 43. What is the use of Dynamic RAM ? **(PTU, May 2016)**

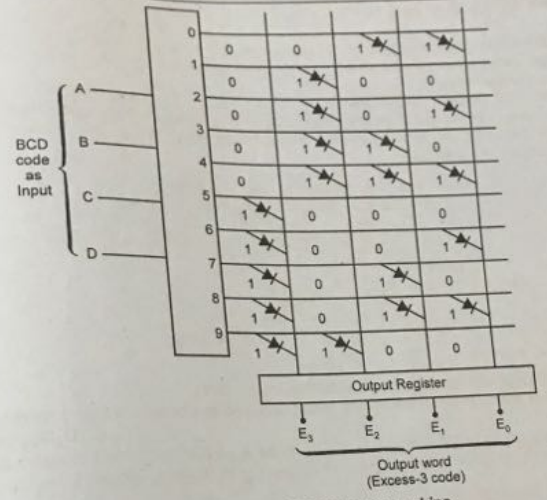
Ans. In DRAM the data will not remain permanently stored unless the data rewritten into memory periodically. It consists of capacitor as memory cell. It uses four MOS transistors. Its power consumption is low as compared to SRAM. Its cost is less and circuit is not complex as compared to SRAM.

Q 44. How does a Dynamic RAM cell works ? Write its applications.
(PTU, May 2019)

Ans. DRAM cell in known as dynamic RAM cell i.e. Dynamic Random Access memory Cell. For its working lets take basic MOS DRAM cell structure as shown in fig.

Typical DRA
and a capacitor is
in MOS capacitor
stored in '1' and
stored is '0'. Whe
i.e. address line,
'C' will be charge
address line go
'C' discharges, t

Applicati
1. DRAM
2. DRAM
3. DRAM
4. DRAM



Q 38. Describe the advantages of CMOS memory chips. **(PTU, May 2014, 2012 ; Dec. 2011)**

Ans. Advantages of CMOS memory chips :

1. CMOS memory chips are faster because of use of both PMOS and CMOS in single chip.
2. CMOS memory chips consumes less power than other MOS families.
3. CMOS memory chips improves noise immunity because of their operation at higher voltages.
4. CMOS chips has very high input resistance and thus, draws almost zero current from the driving gate and hence, its fan-out is very high.

Q 39. What are PROMs? How data can be erased from PROM? (PTU, Dec. 2011)

Ans. Programmable ROM is a ROM into which data is permanently stored by special programming device. A PROM can be programmed once after its fabrication. However another category of PROM is reprogrammable i.e. it can be programmed again and again and is referred erasable and programmable.

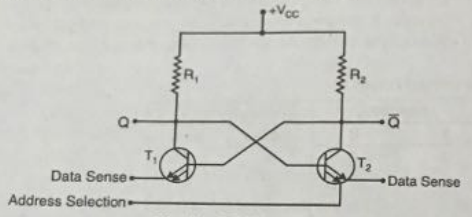
If the erasing of PROM is using ultraviolet then it is EPROM i.e. Erasable programmable ROM.

If the erasing of ROM in using electrical voltage then it is known as electrically alterable ROM i.e. EAROM.

6. Larger flexibility can be achieved using PLA over ROM.
7. Less space is required for designing the circuits.

Q 36. Draw the circuit of a BJT RAM cell and explain its functioning with reference to read and write operation. **(PTU, May 2016 ; Dec. 2012, 2010)**

Ans. Basic Bipolar SRAM Cell : It is as shown in Fig.



Bipolar SRAM Cell

It consists of two BJT's (Bipolar Junction Transistors) having multiple-emitters. When 'T_1' is ON, data sense is '1' and at that time 'T_2' will be OFF i.e., data sense is '0' and vice-versa. This gives two stable states to store data or information in the form of latch. The emitters of T_1 and T_2 except data sense inputs are connected together for addressing to active the cell.

Q 37. Design a diode matrix RAM for conversion of BCD to excess-3 code. **(PTU, Dec. 2011)**

Ans. BCD to excess 3 code using diode matrix RAM is designed from the truth table of BCD to excess-3 code as shown

Decimal Equivalent	BCD Code				Excess-3 Code			
	A	B	C	D	E_3	E_2	E_1	E_0
0	0	0	0	0	0	0	1	1
1	0	0	0	1	0	1	0	0
2	0	0	1	0	0	1	0	1
3	0	0	1	1	0	1	1	0
4	0	1	0	0	0	1	1	1
5	0	1	0	1	1	0	0	0
6	0	1	1	0	1	0	0	1
7	0	1	1	1	1	0	1	0
8	1	0	0	0	1	0	1	1
9	1	0	0	1	1	1	0	0

Here in truth table BCD code ABCD gives the memory location and excess-3 code E_3 E_2 E_1 E_0 gives the bit pattern stored. The implementation using diode matrix RAM is as shown :

/A Convertors

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Approximation type).

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done by using digital to

verter.

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different value resistors

mples.

widely used ADC.

cheaper and gives

QUESTION-ANSWERS

Q 1. Give performance parameters of DAC or D/A converters. **(PTU, Dec. 2012)**

Ans. Resolution : Resolution can be defined in two ways :

(a) A DAC that can provide number of different analog output values is called resolution. For a DAC having n-bits :

Resolution 'R' = 2^n.

(b) A DAC is which the ratio of change in output voltage resulting from a change of 1 LSB (i.e. 1 least significant bit) at the digital inputs is known as resolution.

Resolution for n-bit DAC is given by :

$$\text{Resolution 'R'} = \frac{V_{OFS}}{2^n - 1}$$ Where, V_{OFS} = Full scale output voltage

$$\therefore \text{ Percentage Resolution '\% R'} = \frac{V_{OFS}}{2^n - 1} \times 100.$$

Input-output equation can also be obtained for DAC, if resolution is given :

Where, V_0 = Resolution × D

V_0 = Output voltage

D = Decimal value of the digital input.

If $V_0 = R$, when R = Resolution. Then, % Resolution $= \frac{R}{R\left(2^n - 1\right)} \times 100 = \frac{1}{2^n - 1} \times 100$

2. Accuracy : It is defined as the difference between the actual analog output and the expected analog output when a given digital input is applied. It is expressed in percentage. In ideal case, the accuracy of DAC should be, at worst, $\pm\frac{1}{2}$ of its LSB.

$$\text{Accuracy} = \frac{V_{OFS}}{2\left(2^n - 1\right)}$$

3. Conversion Time or Setting Time : It is the time required for conversion of analog signal into its digital equivalent. It is dependent on amplifiers output and switches response time.

4. Stability : When all the parameters such as gain, linearity error, monotonicity and offset must be specified over the power supply ranges and full temperature then these parameters represent the stability of the converter.

5. Monotonicity : If a converter does not miss any step backward during its entire range stepped by a counter then it is said to have a counter having good monotonicity.

Chapter 7

A/D & D/A Convertors

Contents

Analog & Digital signals. sample and hold circuit, A/D and D/A conversion techniques (Weighted type, R-2R Ladder type, Counter Type, Dual Slope type, Successive Approximation type).

POINTS TO REMEMBER

- The process of conversion from an analog data to digital is done by using analog to digital converter i.e. A/D or ADC.
- The process of conversion from an digital data to analog is done by using digital to analog converter i.e. D/A or DAC.
- Types of DAC's are :
  (a) Binary weighted resistor DAC
  (b) R-2R ladder DAC.
- The R-2R ladder DAC is the most popular digital to analog converter.
- The resolution of DAC is the defined as the smallest change that occur in the analog output as a result of the change in the digital input.
- The disadvantage of weighted resistor DAC is that number of different value resistors are required for each bit position of the digital input.
- Types of ADC's are :
  (a) Flash-type ADC
  (b) Single-slope ADC
  (c) Dual-slope ADC
  (d) Continuous counter type ADC
  (e) Successive-approximation type ADC.
- Quantization is the process of approximation used in digitizing samples.
- Counter type is the simplest ADC and flash type is the fastest.
- The most popular application of ADC is in digital voltmeters.
- The successive-approximation ADC is the fastest and is the most widely used ADC.
- The dual-slope ADC is the slowest type but at the same type it is cheaper and gives excellent accuracy.

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(PTU, May 2015)
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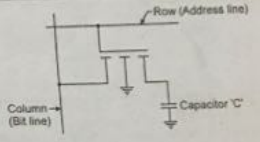
ations.
(PTU, May 2019)
dom Access memory
in fig.

Typical DRAM cell using single MOS transider and a capacitor is as shown in fig. The data in stored in MOS capacitor 'C' when 'C' is charged the data stored in '1' and when 'C' is discharged the data stored is '0'. When storage cell is selected by a row i.e. address line, the MOS conducts and capacitor 'C' will be charged, thus in stores '1' Similarly, when address line goes low, MOS opens and capacitor 'C' discharges, thus stores '0'.



Applications :

1. DRAM is widely used in memory chips where high and low cost clips are required.
2. DRAM in used in modern computers and graphics cards.
3. DRAM is used in cell phones.
4. DRAM is used in global positioning systems.

❑❑❑

Q 6. Name the most popular DAC. **(PTU, May 2009)**

Ans. The most popular DAC is the R-2R ladder DAC.

Q 7. Define the term resolution of an A/D converter.

(PTU, May 2015, 2012 ; Dec. 2007)

Ans. Resolution is defined as the ratio of a change in value of input voltage i.e. V_i, needed to change the digital output by 1 LSB. If the full scale input voltage is V_{iFS} then resolution is given by :

$$\text{Resolution} = \frac{V_{iFS}}{2^n - 1}$$

Where, n is number of bits of A/D converter.

Q 8. Define the term resolution of a D/A converter. **(PTU, Dec. 2007)**

Ans. Resolution : The resolution of D/A converter is defined as the change in the analog output when there is smallest change in the binary input.

For n-bit D/A converter :

$$\text{Resolution} = \frac{\text{Full scale output}}{2^n - 1}$$

Q 9. Define the accuracy of D/A converter. **(PTU, May 2007)**

Ans. Accuracy of D/A converter : The accuracy of the converter is the measure of difference between the actual analog output voltage and the expected output voltage. It is also expressed as a percentage of a full scale or maximum output voltage.

For example :

If an 8-bit D/A converter has weightage of $\frac{1}{2^8}$ to the LSB i.e. 0.0039 or 0.39% of maximum output voltage. The accuracy should be approximately ± 0.2%.

Q 10. Which type of A/D converter is faster and why? **(PTU, May 2015, 2007)**

Ans. Flash type analog to digital converter is the fastest A/D converter. The conversion time for an 'n' bit A/D converter is equal to the 'n' clock cycle period. Thus, conversion time is very short. Hence it is the faster A/D converter.

For example : For a 10 bit A/D converter with a clock frequency of 1MHz, the conversion time will be 10×10^{-6} i.e. 10 μ sec only.

Q 11. What is the need of converting digital data into analog data?

(PTU, Dec. 2005)

Ans. The digital representation of a signal makes storage, processing simpler and its transmission is much easier. Once the transmission and processing etc. is done, the signal we need should be in analog form. To convert the digital signal to its analog form. Digital to analog conversion is required.

Q 12. Why do we need D/A technologies? **(PTU, May 2005)**

Ans. D/A techniques are used whenever, the output of given system is required to be in

. Define its resolution.

zero.

ADC. When input is

alculate the output if

V_{out}

Let I_0, I_1, I_2 and I_3 be the currents flowing through the respective resistors. The value of currents are :

$$I_0 = \frac{V}{R_0} = \frac{0}{5 \times 10^3} = 0$$

$$I_1 = \frac{V}{R_1} = \frac{5}{2.5 \times 10^3} = 2 \text{ mA}$$

$$I_2 = \frac{V}{R_2} = \frac{5}{1.5 \times 10^3} = 3.33 \text{ mA}$$

$$I_3 = \frac{V}{R_3} = \frac{5}{10 \times 10^3} = 0.5 \text{ mA}$$

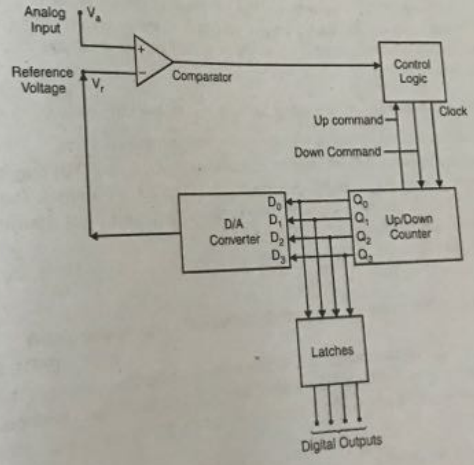
As, the op-amp has a very high input impedance. Thus, the currents I_0 to I_3 flow through 1KΩ resistance.

$$V_{out} = -(2 + 3.33 + 0.5) \times 10^{-3} \times 1 \times 10^3$$
$$= -(5.83)$$

$\therefore$ $V_{out} = -5.83$ volt.

Q 5. Draw only the block diagram of continuous counter type ADC.

Ans.



Block diagram of countiuous counter type ADC.

Q 2. An 4 bit D/A converter has an output range of 0 to 1.5 V. Define its resolution.

Ans. Given :

$n = 4$ = number of bits

Full scale output $V_{OFS} = 1.6$ V

1. Resolution :

$$R = 2^n = 2^4 = 16$$

Thus the output voltage can have 16 different values including zero.

2. Resolution :

$$R = \frac{V_{OFS}}{2^n - 1} = \frac{1.5}{16 - 1} = \frac{1.5}{15}$$

$$R = \frac{100\text{ mV}}{1\text{ LSB}}$$

Thus, an input change of 1 LSB changes the output by 100 mV.

Q 3. Calculate the step size and analog output for 8-bit ADC. When input is 10000000. Reference voltage V_r = +50V is given.

Ans. Given :

$n = 4$ no. of bits

$V_{OFS} = +50$ V

Resolution : $\frac{V_{OFS}}{2^n - 1} = \frac{50}{2^8 - 1} = \frac{50}{255}$

$\therefore$ $R = 0.196$ V/LSB

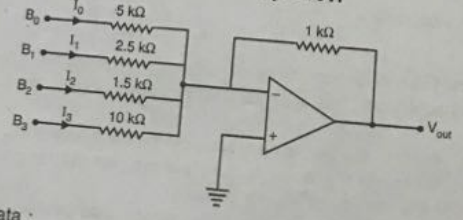
For $V_0 = R \times D$

$\therefore$ $D = (1000\ 0000)_2 = (256)_{10}$

$V_0 = 0.196 \times 256$

$= 50.176$ V.

Q 4. Following fig. shows the D/A converter with op-amp. Calculate the output if the input digital signal is 1110. Assume 1 binary = +5V.

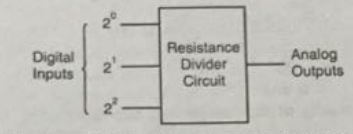


Ans. Binary data :

$B_3\ B_2\ B_1\ B_0 \Rightarrow 1110$

Q 18. With the help of neat diagram explain working of weighted resistor type DAC. **(PTU, May 2016, 2009)**

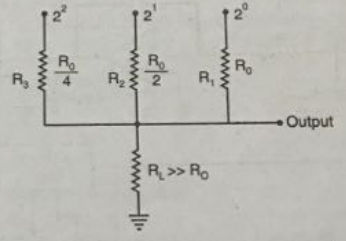
Ans. Weighted Resistor type DAC : Its functional block diagram is as shown for 3 bit input data :



Let us assume that the digital input levels are 0 = 0V and 1 = +7V. Thus, for input 001 the output will be +1V, for 010 the output will be +2V and so on.

For 011, if +1V from 2^0 bit is added to the +2V from the 2^1 bit, the output will be +3V. Thus, 011 input will be achieved.

The internal strcuture for 3 bit digital input and an analog output is as shown :

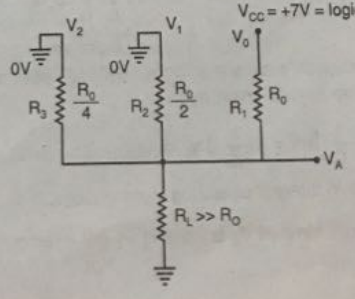


It can be solved by using Millman's theorem, by using formula

$$V = \frac{V_1/R_1 + V_2/R_2 + V_3/R_3 + ...}{1/R_1 + 1/R_2 + 1/R_3 + ...}$$

Let us take an example : If the digital data is 001.

Lets assume that, 0 = 0V and 1 = +7V. Thus, the circuit changes to :



A/D converters are classified into two general groups based on the conversion techniques.

One technique involves comparing a given analog signal with the internally generated reference voltages. This group includes :

1. Successive approximation A/D converter
2. Slope type A/D converter (single slope and dual slope)
3. Delta modulated (DM) A/D converter
4. Adaptive delta modulated A/D converter
5. Flash type A/D converter.

Another technique involves changing an analog signal into time or frequency and comparing these new parameters against known values. It includes :

1. Integrator A/D converter
2. Voltage to frequency A/D converter.

Q 16. Discuss the advantage of binary ladder network over a binary weighted register chain in D/A converter. **(PTU, Dec. 2012, 2005)**

Ans. Advantages of binary ladder network over binary weighted resistor chain in D/A converter :

1. Only two values of resistors are used i.e. R and 2R. So, its construction is easy.
2. Number of bits can be increased by adding more values of R and 2R resistors.
3. R-2R ladder can be fabricated monolithically.
4. Current flow in case of R-2R ladder network is much easier as compared to binary weighted resistor DAC.

Q 17. A certain 12 bit BCA D/A conventor has a full scale output 9.99 V. Determine the percent resolution. **(PTU, May 2005 ; Dec. 2004)**

Ans. Given, $n = 12$,

$V_{FS} = 9.99$ V

(i) Percentage resolution :

$$\% \text{ resolution} = \frac{V_{FS}}{2^n - 1} \times 100$$

$$= \frac{9.99}{2^{12} - 1} \times 100$$

$$= \frac{9.99}{4096 - 1} \times 100 = 0.244\%$$

(ii) Converter's step size :

$$\text{Step size} = \frac{V_{FS}}{2^n}$$

$$= \frac{9.99}{2^{12}} = \frac{9.99}{4096}$$

$$= 0.002439 \text{ or } 2.44 \times 10^{-3}$$

$\therefore$ Step size = 2.44 mV.

analog form then the digital inputs are fed to D/A converter to get back the original analog signal. It is of basic two types :

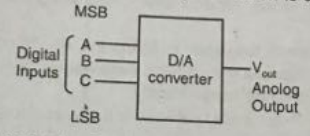
1. Binary weighted resistance D/A converter.
2. R-2R ladder D/A converter.

Q 13. Why we need A/D techniques? **(PTU, Dec. 2004)**

Ans. Most of the information carrying signals such as current, charge, temperature, voltage, pressure and time are available in the analog form. However, for processing, transmission and storage purposes, it is more convenient to express such signals in the digital form. The analog to digital converter is used to convert the analog signal to its digital form which provides better accuracy and reduced noise. Hence, need of A/D converters are essential.

Q 14. Explain about D/A conversion techniques. **(PTU, Dec. 2006)**

Ans. D/A Conversion techniques : Digital to analog conversion is the process of taking a value represented in digital code and converting it to a voltage or current which is proportional to the digital value. Symbolic representation is as shown :



It is a 3 bit D/A converter. Symbolic representation voltage output V_{out} is as shown in table :

A	B	C	V_{out}
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

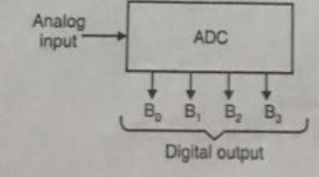
The digital inputs A, B and C are derived from the output register of a digital system. The $2^3 = 8$ different binary numbers represented by these 3 bits are listed in table. For each input numbers, the D/A convert output voltage is a unique value.

The conversion of digital signal to corresponding analog signal can be achieved by using different D/A conversion techniques such as :

1. Binary weighted resistance D/A converter
2. R-2R ladder D/A converter.

Q 15. Explain about A/D conversion techniques. **(PTU, May 2006)**

Ans. A/D Conversion Techniques : In case of A/D conversion analog signal is converted to its equivalent digital form i.e. in binary word.



Q 22. Which is the fastest ADC among available ADCs? **(PTU, Dec. 2009)**

Ans. Flash type A/D converter is the fastest ADC. Because its conversion time is very short.

Q 23. Find %age resolution of a 12 bit BCD input D/A converter which has full scale o/p of 29.97 V. **(PTU, May 2010)**

Ans. Given, $n = 12$

$V_{FS} = 29.97$ V

$$\% \text{ resolution} = \frac{V_{FS}}{2^n - 1} \times 100$$

$$= \frac{29.97}{2^{12} - 1} \times 100$$

$$= \frac{29.97}{4096 - 1} \times 100 = 0.7318\%.$$

Q 24. What technique needs to be used for A/D if the input signal (analog) is changing too fast? **(PTU, Dec. 2010)**

Ans. Flash type A/D converter should be used.

Q 25. List the various A/D convertors. **(PTU, May 2016, 2011 ; Dec. 2016, 2010)**

Ans. Various A/D converters are :

(i) Flash-type ADC
(ii) Single Slope ADC
(iii) Dual-slope ADC
(iv) Continuous Counter Type ADC
(v) Successive Approximation Type ADC.

Q 26. Draw the circuit of a 4 bit D/A (R-2R) convertor and explain how this circuit converts digital data to analog. **(PTU, May 2014 ; Dec. 2010)**

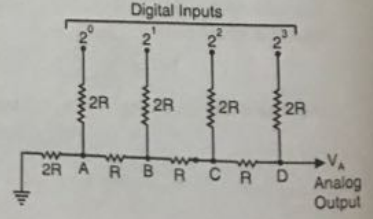
OR

With help of neat diagram explain working of R-2R ladder type DAC. **(PTU, Dec. 2012, 2009)**

Ans. R-2R Ladder D/A Converter : It overcomes the drawbacks of resistive network in which different values of resistances are used. R-2R ladder make use of only two values of resistor i.e. R and 2R. It is as shown in fig.

It uses the formula

$$V_A = \frac{V_0 2^0 + V_1 2^1 + V_2 2^2 + V_3 2^3 + \ldots\ldots}{2^n}$$



Lets take as exar
If digital data is 0
and logic 0 = 0V
logi
n = Number of bi
Here, n = 4 (as c

$V_A = \frac{V_0 \times 2^0 + V}{}$

$V_A = \frac{16 \times 1 + 0 \times}{}$

$V_A = \frac{16 + 64}{16} =$

Thus, the analc
Similarly, if give

Thus, analog

Q 27. Draw th

Ans. Continu
make use of D/A c
1. D/A conve
2. Comparat
3. Up-down
4. Control lir
5. Latches.
It is as show

Let the output of integrator be zero and initially the counter be reset i.e. starts from 0000 (for 4 bit counter). A positive analog input voltage V_{in} is applied through electronic switch S, we get a ramp output and the counter starts counting. When the counter reaches a specified count, it will be reset again and the control logic switches to the negative reference voltage (i.e. $-V_{ref}$) by switch 'S'. At this instant the capacitor 'C' is charged to a –Ve voltage '–V' proportional to analog input voltage V_i. When $-V_{ref}$ is connected, the capacitor 'C' starts discharging linearly due to constant current from $-V_{ref}$. The output of integrating amplifier is non a positive fixed slope ramp which starts at '–V'.

As the capacitor discharges the counter starts from reset state when the output of integrator becomes zero, due to which the comparator output becomes low and it disables CLK through AND gate . Thus, the counter stops and the digital output can be obtained from latches. This completes one conversion cycle. The binary count is proportional to analog input V_{in} or V_i.

Q 20. Find the output voltage from a 5-bit ladder that has a digital input of 11010. Assume that 0 = 0V and 1 = +10V. **(PTU, Dec. 2007)**

Ans. For 5 bit ladder having input of 11010 the output voltage is given by :

$$V_{out} = 10\,[1 \times 2^{-1} + 1 \times 2^{-2} + 0 \times 2^{-3} + 1 \times 2^{-4} + 0 \times 2^{-5}]$$

$$= 10\left[\frac{1}{2} + \frac{1}{4} + 0 + \frac{1}{16} + 0\right]$$

$$= 10\ (0.8125)$$

$$\therefore \quad V_{out} = 8.125\ V.$$

Q 21. For a 4 input resistive divider, find
(i) The full scale output voltage.
(ii) The input voltage change due to LSB.
(iii) The analog output voltage for a digital input of 1011.
Assume 0 = 0V, and 1 = +10V. **(PTU, May 2007)**

Ans. (i) The full scale input voltage :

$$V_{FS} = 10\,[1 \times 2^{-1} + 1 \times 2^{-2} + 1 \times 2^{-3} + 1 \times 2^{-4}]$$

$$= 9.375\ V$$

(ii) The input voltage change due to LSB :

$$V_0 = V_R\,[d_1\,2^{-1} + d_2\,2^{-2} + d_3\,2^{-3} + d_4\,2^{-4}]$$

For LSB calculation, LSB should be high only
thus, 0001 will be the digital input

$$V_0 = 10\,[0 + 0 + 0 + 1 \times 2^{-4}]$$

$$= 0.625\ V$$

(iii) The output voltage for digital input 1011 :

$$V_0 = K\,V_{ref}\,[d.2^{-1} + d_2\,2^{-2} + d_3\,2^{-3} + d_4\,2^{-4}]$$

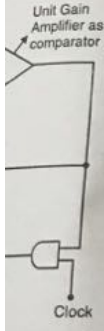
Let $K = 1$

$$V_0 = 10\,[1 \times 2^{-1} + 0 + 1 \times 2^{-3} + 1 \times 2^{-4}]$$

$$\therefore \quad V_0 = 6.875\ V.$$

, May 2017 ; Dec. 2008)
is used because it is free

called dual slope because
fig.



learly shown in fig.

onstant we get an

s well as variable

According to Millman's theorem :

$$V_A = \frac{V_0/R_0 + V_1/(R_0/2) + V_2/(R_0/4)}{1/R_0 + 1/(R_0/2) + 1/(R_0/4)}$$

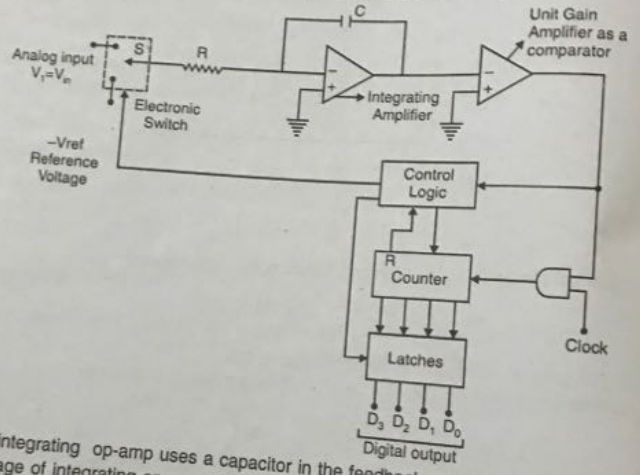
Or
$$V_A = \frac{7/R_0 + 0 + 0}{\frac{1}{R_0} + \frac{2}{R_0} + \frac{4}{R_0}} = \frac{7/R_0}{7/R_0} = +1V$$

$\therefore$ $(001)_2 = +1V$ is analog.

Q 19. Explain the working of dual slope A/D converter. **(PTU, May 2017 ; Dec. 2008)**

Ans. Dual Slope A/D Converter : Dual slope A/D converter is used because it is free from the noise which is not overcome by single slop A/D converter.

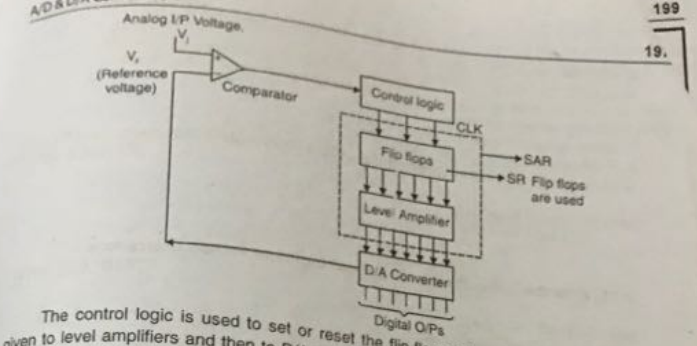
It uses op-amp as integrator amplifier for ramp generation. It is called dual slope because it uses a fixed slope as well as variables slope ramp. It is shown in fig.



The integrating op-amp uses a capacitor in the feedback path as clearly shown in fig. output voltage of integrating op-amp is given by :

$$V_{out} = -\frac{1}{C}\int i\,dt = -\frac{1}{RC}\int V_{in}\,dt$$

Thus, the output voltage in integral of analog input voltage. If V_{in} is constant we get an output $-V_{in}\frac{t}{RC}$. Which is a fixed ramp. If V_{in} is varying we get a ramp fixed as well as variable slope at its output.



The control logic is used to set or reset the flip-flops. The O/P of there flip-flops are given to level amplifiers and then to D/A converter which is a binary ladder network. It gives digital O/P's as well as the analog reference voltage.

Initially the control logic resets all the flip-flops. There are three basic conditions :

1. If $V_r < V_i$ i.e. reference voltage from D/A converter is less than the input analog voltage then MSB (most significant bit) is set to 1 by control logic.
2. If $V_r > V_i$ then MSB is reset to (zero) '0' and next bit is set to '1'.
3. If $V_r = V_i$ then the control logic disables the clock to flip flops and we can get digital O/P from SAR by using latches.

For example : If 4 bit SAR is used.

Let $V_i = 4V$ and let us assume that the counter is reset to zero.

i.e. $V_r = 0$

Now, $V_r < V_i$ MSB is set to '1'

Now, $V_r = 8$ and $V_i = 4$

$V_r > V_i$ next MSB is set and first are reset to zero.

Now, $V_r = 4$ and $V_i = 4$

$V_r = V_i$

Clock is disable by control logic 4 we get 4V as analog voltage is digital O/P 0100

Another example : $V_i = 5V$ and intially $V_r = 0$

Thus, $V_r < V_i$ Ist MSB is set to '1', O/P of SAR = 1000

Again, $V_r = 8V$ and $V_i = 5V$

$V_r > V_i$ Ist MSB is reset to '0' and 2nd MSB is set to '1', O/P of SAR = 0100

Again $V_r = 4V$, $V_i = 5V$

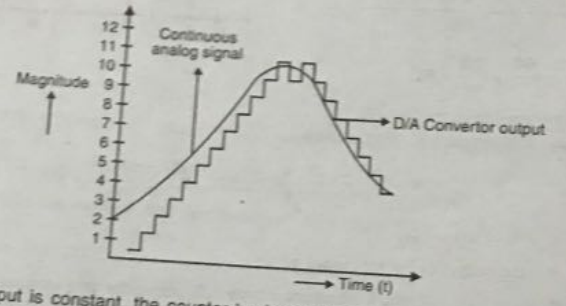
$V_r < V_i$ Next MSB is set to 1, O/P of SAR = 0110

Again $V_r = 6V$, $V_i = 5V$

$V_r > V_i$ 3rd MSB is set to zero and 4th bit is set to '1', O/P of SAR = 0101

Now $V_r = V_i = 5V$ Clock is disabled and O/P of SAR = 0101 is obtained as digital O/P.

The analog input which is to be viewed as digital is given to the comparator i.e. op-amp at its non-inverting input. The output of D/A converter is the reference voltage V_r which is to be compared with the analog input V_i at comparator. If the reference voltage V_r is less than the analog input V_i i.e. $V_r < V_i$, the output of comparator goes High i.e. '1' and due to which the counter is in up mode via control logic. Thus, the counter gives the binary counts and an analog reference output is obtained from the D/A converter which is then compared with the analog voltage V_i. Whenever, the V_r i.e. reference voltage becomes equal to V_i i.e. analog voltage then the output of comparator goes Low i.e. '0' and the counter comes in the down mode through control logic. If the analog input is increasing then the counter starts counting up and if input is decreasing, the counter continues to count back i.e. down. It is as shown in figure.



If the input is constant, the counter backs down on count when a comparison takes place. Due to this backing down on count, the reference voltage V_r becomes a bit less than analog output voltage V_i, the comparator output goes High and count goes to up again. So, if the input is constant, this back and forth action continuous and due to which we get such type of output waveforms.

Q 28. Explain the working of successive approximation A/D converter.
(PTU, Dec. 2015 ; May 2018, 2017, 2016, 2012, 2011)

Ans. Successive Approximation A/D Converter : It is the most widely used A/D converter. It has more complex circuitry than the digital ramp A/D converter but it has much shorter conversion time. For n-bit A/D converter n-successive steps are required for completing the approximation process.

The various functional brakes of successive approximation A/D converter are :

1. Comparator
2. D/A converter (Binary ladder may be used)
3. Control logic
4. Successive approximation register (SAR)

SAR is consists of flip-flops and level amplifiers. It is as shown in fig.

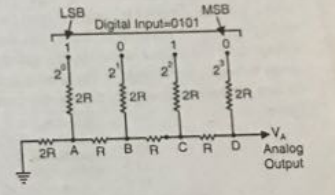
Lets take as example
If digital data is 0101 i.e. 4-bit data
and logic 0 = 0V
logic 1 = +16 V
n = Number of bits.
Here, n = 4 (as data is 4 bit)

(∵ $2^4 = 16$ for 4 bit)

$$V_A = \frac{V_0 \times 2^0 + V_1 2^1 + V_2 2^2 + V_3 2^3}{2^4}$$

$$V_A = \frac{16 \times 1 + 0 \times 2 + 16 \times 4 + 0 \times 8}{16}$$

$$V_A = \frac{16 + 64}{16} = \frac{80}{16} = 5V$$



Thus, the analog output is +5V.
Similarly, if given data is 1000, we have

$$V_A = \frac{0 \times 2^0 + 0 \times 2^1 + 0 \times 2^2 + 16 \times 2^3}{2^4} = \frac{16 \times 8}{16} = 8V$$

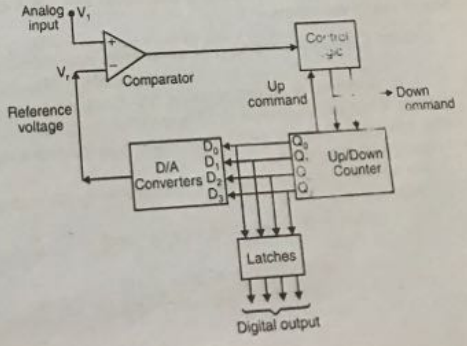
$V_A = 8V$.
Thus, analog output is 8V for binary 1000.

Q 27. Draw the circuit of a 4 bit counter type A/D converter and explain its working. (PTU, May 2013 ; Dec. 2013, 2010)

Ans. Continuous Counter A/D Converter (or up/down) Counter A/D Converter : It make use of D/A converter in it. The main components of this converter are :

1. D/A converter
2. Comparator
3. Up-down counter
4. Control limit and
5. Latches.

It is as shown in fig.



LORDS MODEL TEST PAPER – 2

Instruction to Candidates :

1. Section - A is **Compulsory.** 2. Attempt any **Four** questions from Section - B.
3. Select any **Two** questions from Section - C.

SECTION – A

Q 1. (a) Differentiate between synchronous and asynchronous counters.
(b) What is the function of multivibrator?
(c) Define the term resolution of an A/D converter.
(d) What is a BCD code? What are its advantages and disadvantages?
(e) Realize NAND gate with the help of NOR gates only.
(f) What is full adder?
(g) What are rth's complements?
(h) Name and discuss the various types of semiconductor memories.
(i) Minimize the following boolean expression

$$Y = \left(\overline{A}\,B\,\overline{C} + A\overline{B}\,\overline{C}\right)\left(\overline{A}\,\overline{B}\,C + A\overline{B}\,\overline{C}\right)$$

(j) Explain Moore circuits.

SECTION – B

Q 2. Explain the difference in operation of a monostable and astable multivibrator.
Q 3. (a) Explain the difference between EPROM and EEPROM.
(b) How ROM is different from RAM?
Q 4. With help of neat diagram explain working of R-2R ladder type DAC.
Q 5. (a) State and prove De-Morgan's theorems.
(b) What is race around condition? How it is avoided in Master Slave Flip Flop?
Q 6. (a) Design full subtractor using demultiplexer.
(b) Explain about memory organisation.

SECTION – C

Q 7. Design a comparator circuit which compares two 2 bit numbers. It has three outputs $A > B$, $A < B$ and $A = B$. Also show that $A < B = \overline{A > B} \cdot \overline{A = B}$.
Q 8. (a) Differentiate between static MOS and Dynamic MOS RAM. Draw the circuit of a static MOS RAM cell and explain its working.
(b) Design mod-8 synchronous counter using T flip flops.
Q 9. Write short note on :
(a) MOS digital circuit technology
(b) EPROM memory cell works.

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LORDS MODEL TEST PAPERS

(Unsolved)

LORDS MODEL TEST PAPER – 1

Instruction to Candidates :

1. Section - A is **Compulsory.** 2. Attempt any **Four** questions from Section - B.
3. Select any **Two** questions from Section - C.

SECTION – A

Q 1. (a) What is principle of Duality?
(b) What is the difference between PAL and PLA?
(c) Solve $(10101)_2 - (10011)_2$.
(d) What is the meaning of universal gates?
(e) List the various A/D convertors.
(f) Differentiate between sequential and combination circuits.
(g) What does the term driver mean in a decoder?
(h) What is the 2's complement representation of $(-539)_{10}$ in hexadecimal?
(i) What is shift register?
(j) What is a flip-flop. Draw circuit diagram of D flip-flop?

SECTION – B

Q 2. (a) Define the terms decoder and demultiplexer.
(b) What is multiplexer? Explain with the help of an example.
Q 3. Explain the working of master slave JK flip-flop.
Q 4. (a) Explain FPGA chip.
(b) Draw a logic diagram and waveform for mod – 5 counter.
Q 5. What are multivibrator circuits? Explain Astable multivibrator with the help of circuit diagram.
Q 6. (a) Explain the working of dual slope A/D converter.
(b) Design a mod-6 up counter.

SECTION – C

Q 7. Explain the different types of ROMs. Discuss their advantages and disadvantages.
Q 8. Solve following functionn using Q-M methods and verify the result using K-map. Also implement result using NAND gates only.
$F(v, w, x, y, z) = \Sigma m\ (0, 1, 2, 3, 8, 9, 10, 11, 16, 18, 19, 29, 31)$.
Q 9. (a) Explain the working of successive approximation A/D converter.
(b) Design a MOD-3 synchronous counter using J-K Flip-Flops.

What is DAC? (PTU, Dec. 2012)

Ans. DAC stands for digital to analog converter. The process of conversion from an digital data to analog is done by using digital to analog converter. The converters used for digital to analog conversion are :

1. Binary weighted resistor DAC.
2. R-2R ladder DAC.

Q 30. Determine the resolution of the output from a DAC that has a 12-bit input. (PTU, May 2013)

Ans. Resolution is given by :

$$\text{Resolution} = 2^n$$

$$n = 12$$

$$\therefore \quad 2^{12} = 4096$$

Q 31. Write the name of various types of Digital to Analog Convertors. (PTU, May 2014)

Ans. Types of DAC are :

(i) Binary weighted resistor DAC

(ii) R-2R Ladder DAC.

Q 32. Explain the following :

(i) What is the expression relating the output and inputs of DAC ?

(ii) Define full scale.

(iii) Define percentage resolution

(iv) Accuracy (PTU, Dec. 2015)

Ans. (i) Setling time

(ii) Full scale value is given by

$$FSV = V_{ref} \frac{(2^n - 1)}{2^n}$$

Where, V_{ref} = reference voltage

n = No. of bits of convertor used.

(iii) Percentage Resolution : It is the reciprocal of number of discrete steps in D/A outputs and is given by

$$\% R = \frac{1}{2^N - 1} \times 100 \quad \text{or} \quad \frac{V_{ref}}{2^n}$$

(iv) Accuracy : It is the measure of difference between actual output and expected output. It is given as a percentage of the maximum output voltage.

Q 33. Draw the circuit of R-2R laddder D/A converter and explain its operation. Also determine the resolution of the output from a DAC that has a 12-bit input. (PTU, Dec. 2016)

Ans. Circuit of R-2R laddder D/A converter : *Refer to Q.No. 26*

Resolution of the output from a DAC that has a 12-bit input :

Resolution is given by :

$$\text{Resolution} = 2^n$$

$$n = 12$$

$$\therefore \quad 2^{12} = 4096$$

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LORDS

LO

Instruction to Candidat

1. Section - A is **Con**
3. Select any **Two** q

Q 1. (a) What is principl
(b) What is the diff
(c) Solve $(10101)_2$
(d) What is the m
(e) List the variou
(f) Differentiate b
(g) What does the
(h) What is the 2'
(i) What is shift r
(j) What is a flip-

Q 2. (a) Define the te
(b) What is mult
Q 3. Explain the worki
Q 4. (a) Explain FPG
(b) Draw a logic
Q 5. What are multiv
diagram.
Q 6. (a) Explain the
(b) Design a m

Q 7. Explain the diff
Q 8. Solve following
implement resu
F(v, w, x, y, z)
Q 9. (a) Explain th
(b) Design a